

Chiplet technology for large-scale trapped-ion quantum processors

Bassem Badawi¹, Philip C. Holz², Michael Raffetseder¹, Nicolas Jungwirth¹, Juris Ulmanis², Hans-Joachim Quenzer³, Dirk Kähler³, Thomas Monz^{1,2}, and Philipp Schindler¹

¹*University of Innsbruck, Institute of Experimental Physics,*

Technikerstraße 25/4, 6020 Innsbruck, Austria

²*Alpine Quantum Technologies GmbH,*

Technikerstraße 17/1, 6020 Innsbruck, Austria

³*Fraunhofer Institute for Silicon Technology ISIT,*

Fraunhoferstraße 1, 25524 Itzehoe, Germany

(Dated: December 3, 2025)

Trapped ions are among the most promising platforms for realizing a large-scale quantum information processor. Current progress focuses on integrating optical and electronic components into microfabricated ion traps to allow scaling to large numbers of ion qubits. Most available fabrication strategies for such integrated processors employ monolithic integration of all processor components and rely heavily on CMOS-compatible semiconductor fabrication technologies that are not optimized for the requirements of a trapped-ion quantum processor. In this work, we present a modular approach in which the processor modules, called chiplets, have specific functions and are fabricated separately. The individual chiplets are then combined using heterogeneous integration techniques. This strategy opens up the possibility of choosing the optimal materials and fabrication technology for each of the chiplets, with a minimum amount of fabrication limitations compared to the monolithic approach. Chiplet technology furthermore enables novel processor functionalities to be added in a cost-effective, modular fashion by adding or modifying only a subset of the chiplets. We describe the design concept of a chiplet-based trapped-ion quantum processor and demonstrate the technology with an example of an integrated individual-ion addressing system for a ten-ion crystal. The addressing system emphasizes the modularity of the chiplet approach, combining a surface ion trap manufactured on a glass substrate with a silicon substrate carrying integrated waveguides and a stack of 3D-printed micro-optics, achieving diffraction-limited focal spots at the ion positions.

I. INTRODUCTION

Trapped ions are a promising candidate to realize a scalable quantum computing platform. Recent research in the field shows record qubit gate fidelity [1, 2], long coherence times [3] and the highest quantum volume achieved for any quantum computing platform so far [4]. Error-correcting methods have been applied to protect the quantum information from noise, demonstrating fault-tolerant universal gate sets and state teleportation on the logical qubit level with macroscopic and microfabricated ion trap architectures [5, 6]. Numerous quantum computing applications have been implemented, such as quantum chemistry [7], quantum many-body dynamics [8], combinatorial optimization [9] or quantum machine learning [10].

For quantum computers to become useful for such applications, it is generally believed that more than thousands of qubits are needed [11]. State-of-the-art trapped-ion quantum computers (TIQCs) are inspired by the quantum charged-coupled device (QCCD) architecture [12], where the qubit register is distributed over multiple ion crystals, each acting as a qubit sub-register, and ion crystal reconfiguration techniques are used to achieve all-to-all qubit connectivity [13–16]. However, increasing the amount of ion qubits requires complex processors with high technological demands for the on-chip integration of diverse features [17–19]: i) multi-metal layers and through-substrate vias to enable electrical routing, ii)

material and geometry optimization for low dissipation and high heat conduction, iii) integrated optics for laser light routing and ion addressing spanning wavelengths from deep ultra-violet to the infrared depending on the used ion species, iv) integrated detectors for quantum state readout, v) active and passive electronics and optics for on-chip signal multiplexing and manipulation, and vi) deep and stable trapping potentials, optimally using segmented 3D ion traps [20]. Finally, all technologies and materials should be compatible with cryogenic temperature, that allows one to create the extremely high vacuum needed for reliable storage of large numbers of ions. This plethora of needed features leads to a large fabrication complexity and high costs. Combining all features in a monolithic design furthermore creates conflicting requirements, forcing trade-offs that can adversely affect processor performance.

Stacked wafer technology, which interfaces different components, has been developed as a possible mitigation strategy for these technological obstacles [17, 21]. We extend this idea by proposing a TIQC buildup inspired by the emerging chiplet technology, that uses a system of multiple interfaced chips combined in one package to extend the fabrication possibilities and maximize processor modularity using a divide-and-conquer approach. This chiplet approach shifts complexity from the chiplet fabrication to their packaging. In particular, we propose to realize the ion trap and the integrated optics on individual chiplets, in contrast to state-of-the-art mono-

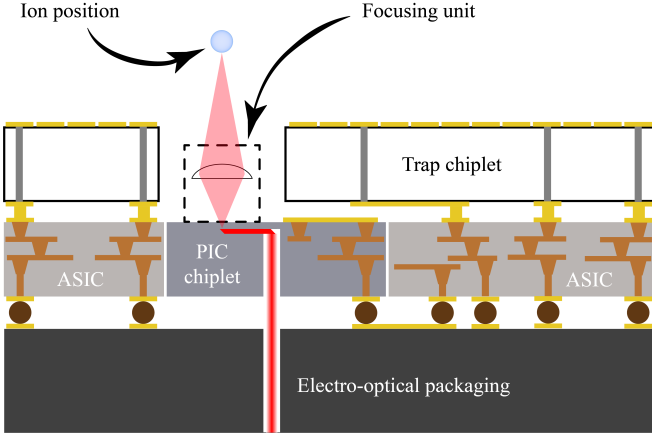


FIG. 1. Illustration of a conceptual chiplet stack forming a SiP as platform for scalable TIQC processors. An electro-optical packaging at the bottom serves as an active interposer for the mounted ASICs and PIC chiplets in the middle layer. ASICs and PIC chiplets are laterally interfaced via the interposer and serve in turn as mounting platform for the trap chiplet and further optical elements, e.g., a focusing unit manufactured in a slotted area of the trap chiplet.

lithic realizations [22–24]. A chiplet approach to optics integration simplifies the individual module fabrication and avoids a common compromise in the choice of chip substrates: the manufacturing of complex TIQC processors [20, 25–27] usually employs silicon as the basic substrate material due to the low adaption efforts when using standardized complementary metal-oxide-semiconductor (CMOS) processes. However, silicon is not well suited for the application in ion traps, and a lot of fabrication complexity is required to avoid RF and photon absorption within the substrate [27, 28]. The fabrication of an ion trap electrode structure on a dielectric substrate material with low RF loss, such as fused silica, crystalline quartz, or sapphire [29–31], simplifies fabrication efforts once the process technology is developed. Using heterogeneous integration technology [32], bare ion trap chips with optimal substrate material may then be interfaced with separately fabricated silicon chips carrying standard optical waveguide platforms [22, 24, 33] and CMOS technologies, e.g., photon detection [34, 35], active integrated photonics components [36], cryogenic amplifier [37] or digital-to-analog converters (DAC) [38].

We begin this article with an introduction to the chiplet approach and its benefits for the realization of a scalable TIQC processor. We then demonstrate the realization of a building block for individual ion addressing using chiplet technology, before we conclude by pointing out future prospects for the use of the chiplet approach for TIQC processors.

II. CHIPLET APPROACH FOR TIQC PROCESSORS

In the traditional semiconductor industry, the functionality of a central processing unit (CPU) relies heavily on the density of transistors on a single chip. However, this relationship comes at the cost of increased fabrication complexity and immense processing expenses. Gordon Moore examined the relationship between relative fabrication costs and the number of components per integrated circuit (IC), which is now known as Moore’s Law. [39, 40]. Rather than increasing system complexity through constant feature size reduction, the ”More than Moore” approach incorporates additional functionalities, such as RF communication, power control, passive components, sensors, and actuators, on separately fabricated chiplets. The integration of multiple chiplets on a common interposer, along with their interconnection, forms a system-in-package (SiP) [41] with a functionality similar to or higher than that possible with monolithic integration alone.

The ”More than Moore” movement [42] developed a concept that enables more modular architectures and offers significant technological improvements over monolithic architectures. This concept can be applied to realize a large-scale TIQC processor, where all functionalities are integrated into several chiplets, offering substantial advantages: i) The fusion of multiple manufacturing technologies and materials in a SiP offers the ability to pick the technology that is best suited for different functionalities in the TIQC processor; ii) Parts of the SiP can be revised or modified without having to adapt other system components iii) The modular construction may lead to more reliable sub-components and significantly faster and more cost-efficient development iterations compared to monolithic integrated TIQC solutions, where revisions typically require complex adjustments in the overall manufacturing process.

Here, we describe a modular SiP architecture for a TIQC processor that consists of multiple chiplets which are placed and interfaced laterally and vertically, as illustrated in Fig. 1. The top layer is reserved for the ion trap (henceforth named trap chiplet), which comprises a substrate material with low RF loss, electrodes on the chiplet top surface for ion trapping, through-substrate vias (TSVs) to connect the electrodes with the chiplet back side, and openings in the substrate for optical access. These openings can be used to host microfabricated optical elements that act as focusing units. The second layer comprises multiple supply chiplets for photonic and electric signal routing and control. Chiplets with photonic integrated circuits (PICs) are used to route and switch optical signals [36], supplying the laser light for photoionization, laser cooling and qubit control to the ion trapping locations. Chiplets with application-specific integrated circuits (ASICs), for instance integrated DACs [38] or switch-matrices [43], are used to route and control the electrical signals for ion trapping and transport op-

erations. The third and bottom layer serves as an active interposer [44] for the chiplet stack. Besides electrical interfaces commonly used to connect the trap electrodes to electrical supply lines [45], the package may also integrate an optical interface to optical fibers connected to the supply laser, thus forming an electro-optical package. The packaging layer furthermore thermally anchors the chip stack via an attached heat sink.

Bonding or soldering processes are used to mechanically and electrically interface the individual chiplets. Possible options encompass metal bonding [46], hybrid-bonding [47], and solid-liquid interdiffusion (SLID) bonding [48], as well as low-temperature soldering using tin, bismuth, or indium alloys [49]. The applicable thermal budget, possible surface preparation, and interconnect density determine which bonding or soldering technology is suitable for SiP chiplet interconnections. The interfacing necessitates its own process developments and plays a key role in the packaging complexity.

We stress that the chiplet approach, due to its inherently modular nature, goes beyond mere chip stacking. For example, it is challenging to combine PIC and ASIC components monolithically in a single chiplet due to lithography restrictions, contamination issues, or incompatible manufacturing processes. However, such technological limitations can be completely avoided by using separate PIC and ASIC chiplets, as illustrated in Fig. 1, each fabricated using distinct fabrication technologies tailored to the respective chiplet functionality. Likewise, the first SiP layer may comprise several trap chiplets. Furthermore, additional components can be integrated in between two chiplets or in chiplet openings, such as the additional optical elements described in section III.

A. Example realization

Several architectures for a scalable TIQC processor have been proposed: a quantum charge-coupled device [12], a quantum spring array [16], processors employing magnetic gradient induced coupling [50] or network approaches using photonic interconnects [51]. For all of these architectures, typically a monolithic integration approach has been considered. However, they can likewise be realized with the chiplet approach, as we will illustrate at the example of a QCCD-type processor. The example TIQC SiP we consider is illustrated in Fig. 2. The ion trap design on the SiP top layer is an array of linear trap sections connected by X-junctions, as envisioned in several previous works, e.g. [21, 52]. The magnified view on the left shows a trap region around one of these junctions. Out of the four linear trap "arms" leaving this junction, one arm serves as a laser addressing zone for qubit manipulation using integrated waveguide technology with additional optical elements, while a second arm carries an integrated photon detector for qubit state detection. The other two arms serve as storage zones and all four

arms are connected to adjacent parts of the trap array. A register of ion-qubits can be trapped in such an array using a combination of radio-frequency (RF) and direct current (DC) voltages [53] applied to the trap electrodes. The qubit register is thereby distributed over multiple sub-registers. Each sub-register comprises a small number of ions stored in an individual trapping well which can be transported between the different zones of the trap array by adjusting the DC voltages on the trap electrodes. The wells can also be split and merged to enable quantum gate operations between qubits originally in different wells [14].

As illustrated in the conceptual cross section in Fig. 1, the TIQC-processor in Fig. 2 consists of separately manufactured chiplets that are electrically and optically interconnected using heterogeneous integration technology [32]. The trap chiplet carries the RF and DC trap electrodes on a dielectric substrate, which offers beneficial properties with respect to RF loss. Metalized through-substrate vias (TSVs) interconnect the front side of the trap chiplet to its back side. The PIC chiplet on the second layer is fabricated on a silicon substrate to benefit from the standardized production of classical integrated circuits (ICs) and photonic integrated circuits (PICs). In our example realization, the PIC chiplet carries optical waveguides for integrated laser routing and a top metal layer to serve as an additional redistribution layer (RDL) of electrical signals. Microfabricated optical elements are integrated into a trap chiplet trench. These optical elements focus laser radiation emitted from the waveguides onto the ion positions. For this reason, this optical system is named the "focusing unit". As depicted in Fig. 1, the second layer may consist of multiple chiplets to increase the functionality of the SiP. Metal or metal-oxide hybrid bonding technologies establish an electrical contact between the trap chiplet back side metal and the PIC chiplet front side metal. The overall chiplet stack is bonded using flip-chip technology on a PCB interposer, which forms the third layer. Optical signals are interconnected by a fiber-to-chip edge coupling technique to the PIC chiplet. Next generation optical interfaces shall be provided through the electro-optical packaging as envisioned in Fig. 1.

B. Technological advantages

The realization of a TIQC processor using chiplet technology offers several advantages over monolithic integration with respect to signal routing, power dissipation, and heat management of the processor, and integration of passive and active electronic components enhancing the processor performance. The proposed chiplet technology breaks with the established monolithic integration in that the TIQC processor no longer relies on a specific chip manufacturing technology, e.g., CMOS-compatible semiconductor technology or photonic waveguide technology. This provides significant flexibility in selecting

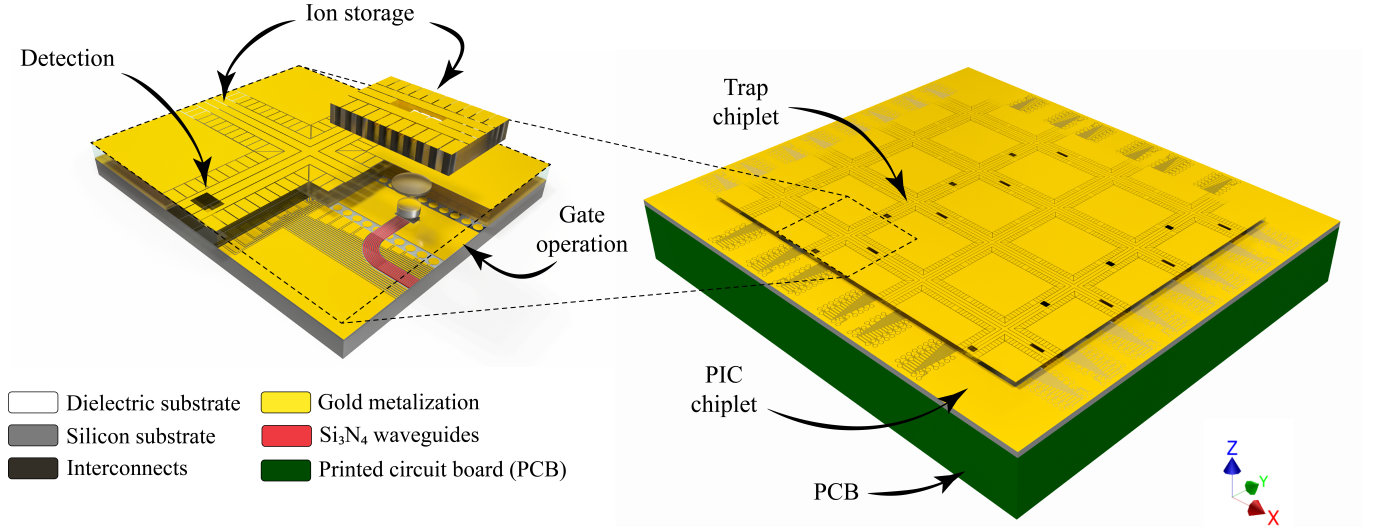


FIG. 2. Illustration of a QCCD-type TIQC processor constructed with chiplet technology introduced in Fig. 1. The SiP consists of a trap chiplet bonded onto a PIC chiplet and interfaced on a electro-optical package used for the signal fan-out to peripheral system components. The chiplet stack is mounted via standardized flip-chip bonding technique onto the electro-optical package. Interconnects between dielectric and silicon substrate are created via TSVs and metal-metal bonding technology. The magnified view on a single X-junction on the right shows the parts of the SiP necessary for the required ion transport and qubit operations in a large-scale TIQC processor. Parts of the trap chiplet are cut off to provide open view on the optical and electrical signal fan-out and ion addressing zone.

the most appropriate manufacturing techniques for specific components of the TIQC processor and can also speed up development iterations, albeit at the cost of increasing packaging complexity. In general, technologies and realizations can be transferred from monolithically integrated ion traps in a SiP, though this is not always straightforward and can require design changes.

Specifically, the integration of optical elements for the ion addressing differs from known monolithic techniques that use grating couplers or metasurfaces to focus laser beams [22, 33, 54, 55]. With the commonly used focusing grating couplers, it is challenging to realize single-ion optical addressing in longer ion crystals [56] due to the large footprint per optical channel. This issue can be solved by using microfabricated lenses, which focus multiple optical channels with the same optical element. Due to the modular nature of the chiplet approach, the integration of such elements is much simpler in a SiP than it would be in using monolithic integration.

Many developed components of monolithic ion traps with integrated optics, e.g. the entire trap electrode design or PIC elements such as optical beam splitters, can be integrated into a SiP without required design changes. In the following subsections, we concentrate on components in a TIQC processor that can be enhanced using the proposed chiplet architecture.

Ion trap substrate

The separation of the ion trap chiplet in the first layer from the PIC and ASIC supply chiplets in the second layer allows one to select the optimal substrate material for the ion trap chiplet. From a trap performance point of view, the key properties of a good substrate are electrical insulation, low RF loss, large bandgap, and high thermal conductivity. The realization of the trap chiplet on a fused-silica substrate, in combination with TGVs, fulfills these requirements: In contrast to silicon, dielectric substrates, such as fused silica, have superior electric properties because of their low RF loss tangent with minimal heating from RF dissipation in the substrate. Also, due to the large band gap compared to silicon, laser radiation absorbed in the bulk does not generate mobile charge carriers, which can enhance RF dissipation and may even lead to uncontrolled ion displacement. For these reasons, traps with silicon substrate typically employ additional metal layers to shield the substrate from RF and laser fields [57]. Such a multi-metal layer stack, if not carefully designed, leads to high trap capacitance [27]. The omission of the shield layer for dielectric substrates allows the capacitance of the ion trap to be significantly reduced, which in turn reduces the RF dissipation of the trap [28].

With respect to the heat management of the ion trap, sapphire or diamond offer high thermal conductivities at cryogenic temperatures, where most ion traps are operated. Additionally, materials with poor heat conductivity, such as fused silica, can be used by exploiting the

heat conductivity of the metal filled TGVs which may provide a high effective thermal conductivity from the trap chiplet front side to the heat sink on the packaging back side.

Electrical signal routing

The electrical signal routing to supply areas is called signal fan-out, and becomes challenging as the TIQC processor scales up to accommodate an increasing number of ions. A single top metal layer cannot provide the required connectivity [4, 28, 58]. Thus, multiple stacked and interconnected metal layers, each acting as an RDL for electrical signals, are required. In monolithic fabrication, the signal routing is usually solved by a single-sided multi-metal layer stack. The chiplet realization in Fig. 2 provides already two RDLs using the metal layers on the back and front side of the trap and PIC chiplets, respectively. The number of RDLs can be further increased using multi-metal layers on either the trap chiplet back side or on the PIC chiplet front side, without significantly adding to the trap capacitance as long as the RF electrodes are only routed on the trap chiplet top side. With the usage of TGVs, low impedance grounding of DC electrodes in the AC domain could be provided by adding small footprint trench capacitors [27, 59] to the PIC chiplet, directly below the DC electrodes.

Optical signal routing

A key technological obstacle for large-scale TIQC processors is the integration of optical components that enable the manipulation of the qubit state as well as state readout and laser cooling at the desired zones of the TIQC processor. The state-of-the-art for on-chip laser routing is the application of standardized waveguide technologies [60] based on distinct material platforms depending on the specific wavelengths for the used atomic species. All readily available waveguide platforms are based on silicon process technology and offer low-loss laser routing and versatile possibilities for the integration of additional passive [61] and active [62] optical components used for signal multiplexing, mode conversion or suppression, optical switching, spot size conversion and optical filtering. The monolithic integration of waveguide technology on dielectric substrates is principally possible but requires extensive process development to establish a waveguide platform on substrate materials other than silicon with optical performances comparable to those of the available technologies. Due to the high costs for the process development of a waveguide platform on a dielectric substrate, monolithic integration of waveguide technology on dielectric substrates will likely not be available in the near future. Heterogeneous integration technology offers the possibility of using advanced waveguide technology in combination with a surface ion trap fabricated

on a dielectric substrate, again with the goal of picking the optimal materials for the individual processor components.

By using a dedicated PIC chiplet for the optical integration of passive and active optical components, the fabrication becomes significantly simpler. The PIC chiplet does not have trap electrodes. With the large separation between silicon material and RF electrodes, and several metal layers in between, the PIC chiplet does not require a shielding layer for the silicon substrate [63]. Transparent conductive materials, e.g., indium-titanium oxide (ITO), are an alternative to shield dielectrics in the laser interaction zones of the ion trap [22, 64, 65]. For the chiplet approach, these additional conductive layers can likely be omitted, because dielectrics are not in close proximity to the ions and are already sufficiently shielded by the trap chiplet top metallization. This simplification of fabrication requirements may facilitate the realization of more complex photonic layers with hybrid material platforms routing laser radiation of a broad spectrum from ultra-violet to infrared [54].

The larger distance between the ion location and the laser out-coupling in the chiplet approach adds the possibility to integrate additional components between the trap chiplet and PIC chiplet to add optical functionality. Examples of this are printed three-dimensional optical elements which enable individual ion addressing of qubit sub-registers, as we will present in section III.

Integrated electronics

Incorporation of advanced functionalities into a scalable TIQC processor can be achieved through the integration of active electronics, e.g. ASICs, on additional chiplets within the SiP. In the context of DC signal management, the utilization of DACs for signal generation [38] or integrated switch matrices for signal multiplexing [43] exhibits considerable potential. Likewise, active photonic components need to be integrated to control the laser phase and amplitude for individual optical channels [36]. Regarding the readout of qubit states, the utilization of integrated photodetectors, including single-photon avalanche diodes (SPADs) [66] or superconducting nanowire single-photon detectors (SNSPDs) [67], is a viable option. However, new strategies for qubit state detection can be explored. A promising approach involves the use of grating couplers or microfabricated lenses to couple ion fluorescence in optical channels of the PIC chiplet that are terminated by integrated detectors. This approach may be combined with integrated beam splitters, to generate ion-ion entanglement [68].

Rapid design modifications and added functionality

The modular nature of the chiplet approach enables faster and more cost-effective prototyping than mono-

lithic integration allows. Revisions to individual system components do not affect SiP chiplets that are not directly interfaced with the revised parts. A typical revision of the SiP represents a change in trap chiplet electrode design, to realize an optimized surface ion trap architecture without the requirement to adapt the PIC chiplet. Similarly, adaptations of the PIC chiplet, such as the addition of optical channels, a change in photonic routing, or a transfer to a different waveguide platform (e.g. from Si_3N_4 to Al_2O_3), do not require an adaptation of the trap chiplet, as the interface remains unchanged. Through this modularity, unrevised SiP components can be fully recycled in the optimized TIQC SiP. New technologies, such as SNSPDs made from high-temperature superconductors [69, 70], can be incorporated into separate chiplets that can be more easily integrated into a functional SiP than a complex, dense integrated chip die. Furthermore, integrating specific functional elements, such as microfabricated lenses, is significantly facilitated with chiplet technology.

III. REALIZATION OF A CHIPLET-BASED TIQC PROCESSOR

We demonstrate the technological advantages of the SiP approach at the example of a TIQC processor building block which enables the optical addressing of single ions in a crystal of ten ions. We choose this building block because, addressing multiple ions is difficult in monolithically integrated realizations relying on focusing grating couplers. In such a system, each ion requires its own output coupler and thus the footprint becomes prohibitively large such that integrating ten or more independent optical channels next to each other becomes challenging [56]. We circumvent this footprint issue by using a microfabricated lens stack, which uses a single focusing element to address all ions, similar to a macroscopic objective [71].

The conceptual design of the qubit addressing building block is shown in Fig. 3a,b. The building block consists of the trap chiplet, which hosts a slotted linear surface ion trap, and is bonded to the PIC chiplet. The slot creates an optical access from the back side of the trap chiplet to the ions, positioned above the RF and DC electrode structure. Individual ions in a linear crystal are addressed with focused laser beams by imaging the output of a waveguide array with a focusing unit consisting of microfabricated lenses placed on top of the PIC chiplet. Each waveguide in the array serves as a dedicated optical channel for one specific ion in the linear ion crystal. The distance between adjacent waveguides corresponds to the ion spacing in a given trapping potential, taking into account the magnification of the focusing unit. The waveguide array terminates at a microfabricated mirror, depicted as metalized ramp, that serves as a deflection element to redirect the laser beams perpendicular to the PIC chiplet surface.

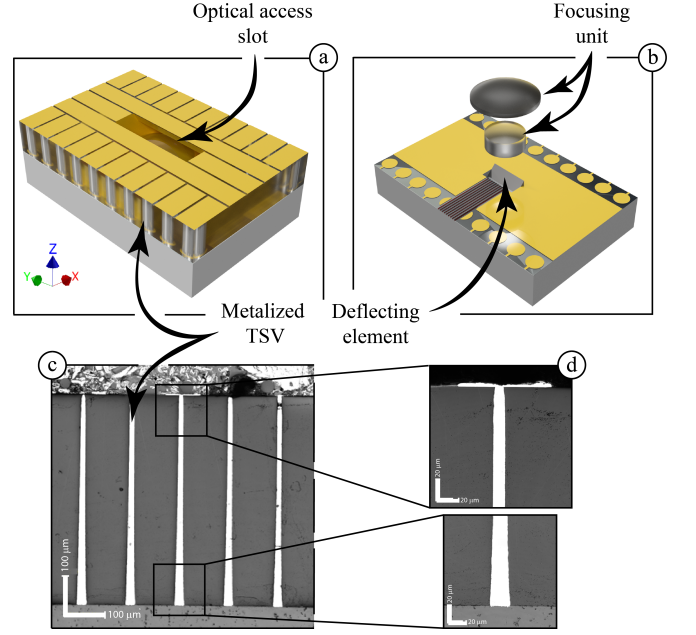


FIG. 3. (a): Illustration of a qubit addressing building block, consisting of a slotted trap chiplet with a glass substrate stacked on a PIC chiplet with a silicon substrate. The slot in the trap chiplet houses an integrated lens stack. (b): Exploded view of the addressing building block without the trap chiplet showing the integrated lens stack that serves as the laser focusing unit. A deflecting element realized on the PIC chiplet redirects the laser beams from waveguides towards the lens stack. (c): Scanning electron microscopy cross section of aluminum filled TSVs electrically interfacing trap chiplet front and back side. (d): Magnified top and bottom part of one TSV, showing no delamination of the aluminum from the substrate after several cool-down cycles to liquid nitrogen temperature.

Ion trap chiplet and electrical routing

For the trap chiplet we employ a borosilicate substrate with gold (Au) electrodes on the front side and an Au routing layer on the back side. We use borofloat glass instead of fused silica due to the better match of the thermal expansion with the silicon substrate of the PIC chiplet. The electrical connection between the back and front side metal layers on the trap chiplet is realized by TSVs, shown in Fig. 3c. A magnified image of a single metalized TSV is shown in Fig. 3d. The demonstrated TSVs consist of high-aspect-ratio cavities produced in the borofloat glass and completely filled with aluminum to ensure electrical conductivity from the back side to the front side metal. The cryo-compatibility of the fabricated TSVs has been tested by cycling the sample structures between ambient and liquid nitrogen temperatures several times. No metal delamination or deformation of the TSV cavities was observed, demonstrating the reliability of the interconnects. We expect that the additional thermal contraction of the TSVs from liquid nitrogen temperature to the operational temperatures of an ion trap

around 10 K is negligible [72].

Integrated addressing building block

A more detailed view of the qubit addressing building block is shown in Fig. 4a-e. Our demonstrator is designed to allow for individual ion addressing of ten $^{40}\text{Ca}^+$ ions in a linear crystal trapped in a single potential well using 729 nm light. A ten ion crystal has an average ion spacing of about 4 μm [73], which requires highly focused addressing beams for single ion addressing. We use microfabricated optical elements printed directly on the Au-surface of the PIC chiplet using two-photon polymerization technology [74]. The optical system, depicted in Fig. 4b and Fig. 4c, is housed in a Au-metalized slot below the laser interaction zone of the trap chiplet and is designed such that each optical channel is imaged onto a corresponding ion position with diffraction limited spot sizes with a numerical aperture of 0.24 and minimized optical crosstalk between adjacent ions.

The printed focusing unit, shown in Fig. 4d, consists of a dielectric material that is likely to induce electric-field noise at the position of the ion crystal, causing motional heating [75]. To minimize ion heating, the imaging distance of the optical system is designed to be as large as possible. The metalized and electrically grounded side-walls of the optical access slot in the trap chiplet additionally shield the ions from stray charges and electric-field noise emanating from the lens stack.

Optical crosstalk between neighboring optical channels is not only generated by the focusing unit but can also occur on the PIC chiplet due to light leakage from neighboring waveguide structures. Optical simulations determine the crosstalk of adjacent waveguides to approximately -30 dB for a waveguide distance of 5 μm . The intensity of crosstalk caused by waveguide leakage is similar to the intensity of the simulated crosstalk caused by the focusing unit. For on-chip laser routing at a wavelength of 729 nm, we employ Si_3N_4 waveguides that are edge-coupled from one PIC chiplet edge. The laser beams in the waveguides are deflected from the PIC chiplet surface plane by total internal reflection (TIR) mirrors, realized directly within the waveguide structures, as shown in Fig. 4e(left). The TIR facet within the waveguide array is created by focused ion beam milling a oblique trench into the $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ layer stack. We employ TIR mirrors instead of the 45° ramp depicted in the conceptual illustration, Fig. 3b.

The laser light guided by the waveguide is reflected upwards at the Si_3N_4 /air TIR-mirror interface and propagates out of the waveguide cladding at an angle to the surface normal depending on the trench angle. The critical angle of the ion milled trench for TIR in this setup is simulated to be approximately 43°.

We fabricate the TIR mirrors at an angle of 52°, resulting in an out-coupling angle $\alpha \approx 20^\circ$ as this angle gives the highest fabrication accuracy. A finite-difference time-

domain simulation of the laser propagation at the TIR mirror structure depicted in Fig. 4e(right) shows the out-coupled intensity distribution. We use a prism structure, indicated in Fig. 4b, printed below the first lens of the focusing unit to correct the light propagation and achieve a perpendicular out-coupling out of the PIC chiplet, minimizing optical aberrations in the focusing unit. The other optical components of the focusing unit are designed to generate elliptical focal spots with high focusing ability in the x-direction and a larger spot size in the y-direction. This elliptical beam shape, with aspect ratio of one two three, ensures minimal optical crosstalk between neighboring ions, but relaxes the requirements for chip alignment accuracy. A dark field microscopy image of the fabricated focusing unit printed onto the TIR mirror position is shown in Fig. 4d.

We have tested the optical performance of the Si_3N_4 waveguide design, the TIR mirrors, and the focusing unit with separately fabricated PIC dies equipped with focusing units identical to the one shown in Fig. 4d. The optical system is designed to have a magnification of 0.6, which determines the required waveguide spacing when addressing a linear crystal of ten $^{40}\text{Ca}^+$ ions. At an axial common mode frequency of the ion crystal of 700 MHz, the required waveguide spacing varies between (4.84-6.62) μm . We determine the magnification of the optical system by balancing optical aberrations originating from the lens stack with crosstalk between adjacent waveguides. We characterize the performance of the building block by measuring spot sizes and focal distances. We couple light into the waveguides using a 6-axis translation stage that holds the PIC chiplet with the printed focusing unit and characterize the spot size of the out-coupled light with a microscope. A typical measurement of a waveguide that illuminates the third outer ion is shown in Fig. 5a,b.

The measurements show a focal spot size in the x-direction of 1.7 μm , and 3.4 μm in the y-direction. The focal spot is measured at a distance of (169 ± 6) μm above the focusing unit, which differs from the simulated value by 8 μm . Taking the Rayleigh length of approximately 13 μm into account, the focal spot size and distance correspond well to the simulated data. The simulation yields a mode-field diameter (MFD) at a focal distance of 177 μm in x- and y-direction to be 1.3 μm and 3.5 μm , respectively. We note that the light propagation angle in the y-direction shows a deviation from the intended propagation normal to the PIC surface. This deviation originates from an incorrectly shaped prism structure below the lens stack which was designed for a TIR angle of 7° while the actual out-coupling angle is 20°. This deviation from the model causes light clipping on the focusing unit in the y-direction. Through further optimization, we are confident that we can match the optical design to the actual out-coupling in an improved version.

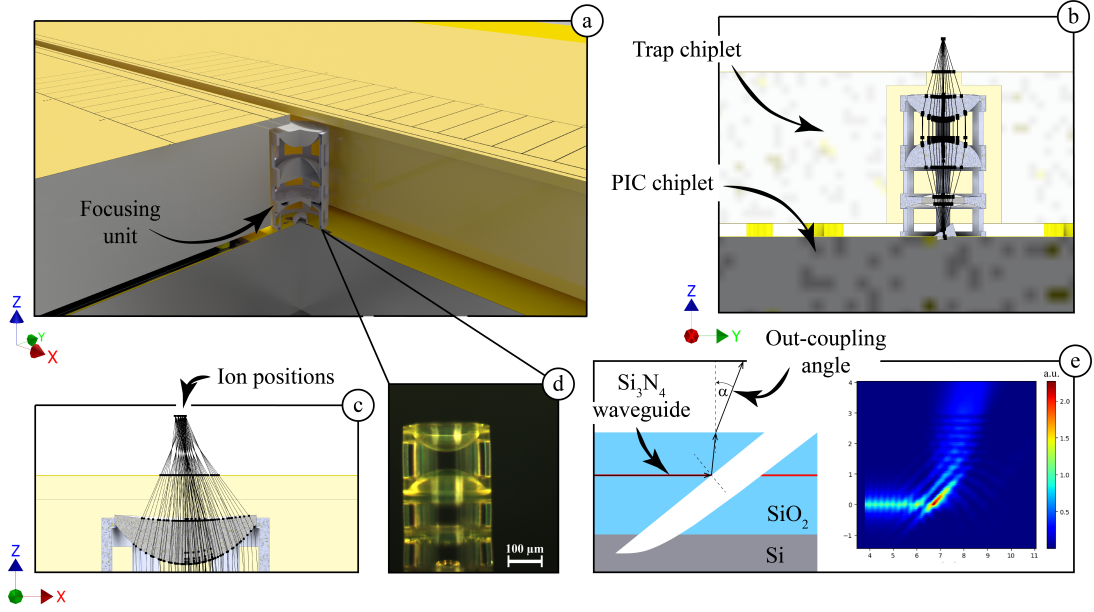


FIG. 4. (a): Demonstrator CAD design of the integrated qubit addressing building block. (b), (c): Half-cuts through the CAD design at the focusing unit position in YZ-plane and XZ-plane, respectively. (d): Microscopy image of a fabricated focusing unit on a PIC chiplet. (e)(left): Illustration of a TIR mirror structure for a single waveguide and pointing vector of the light propagation. (e)(right): Finite-difference time-domain simulation of the light propagation through the TIR mirror structure for a single waveguide.

Chiplet bonding

Finally, we demonstrate the bonding of the trap chiplet to the PIC chiplet, which is a crucial step in fabricating the proposed TIQC SiP. The thermal expansion of the trap and the PIC chiplet substrate materials differs, which causes stress and makes high-temperature bonding technologies unsuitable for interfacial bonding. We therefore employ a low-temperature thermo-compression bond technique. We additionally compensate for the stress resulting from the thermal expansion mismatch of the substrate materials by employing a thick Au-bonding interface of about 20 μm . Typical metal-metal bonding requires a maximum surface roughness of approximately (2-3) nm_{rms} . With a thick galvanic gold layer, this surface roughness specification is the key factor in achieving high-quality bonding at low temperatures. The maximum heat limit during bonding is determined by the polymer material of the focusing unit. Since overheating can cause damage, it's important to keep the bonding temperature below the point at which the carbon compounds in the polymer begin to evaporate. In collaboration with EV Group GmbH, LioniX International BV and Printoptix GmbH we developed an appropriate thick Au metal-metal bonding process compatible with these restrictions. A bonded chiplet stack with a simplified version of the addressing building block without slots in the trap chiplet and without printed lenses is shown in Fig. 6a-c. The bonding process was developed on wafer scale using a 100-mm silicon wafer and a 200-mm borosilicate wafer. The silicon wafer was manufac-

tured using standard silicon material with a SiO_2 layer of 8 μm thickness and a 500-nm thick structured Au layer. The borosilicate wafer was patterned with 20 μm thick Au structures only on its back side. Figure 6a shows an image of bonded chiplet stack after dicing. In Fig. 6b, an x-ray computer tomography (CT) image of the thick Au bonding structures, with a resolution limit of 7 μm , is shown. Micrograph images from the bonding interface are shown in Fig. 6c. On the tested samples, we cannot observe any open interfaces. The zoom-in image of a single bonding structure in Fig. 6c proves an excellent interface between the Au-surfaces, so we expect a high electrical conductivity of these structures, to be verified in upcoming electrical measurements. Several additional CT images and an acoustic microscopy image of the sealing structure are shown in Appendix A. These additional investigations revealed no bonding failures in any of the imaged structures. A defect-free bond is especially important for the sealing structure, visible as rectangle around the chiplet slot, which is intended to enclose the focusing unit in the final chip stack to protect it from water and residues produced during the dicing of the wafer stack. The wedge error between the wafers was not measurable within the measurement resolution of 0.002°.

IV. CONCLUSION AND OUTLOOK

The chiplet architecture presented in this work extends the established paradigm of TIQC processor manufactur-

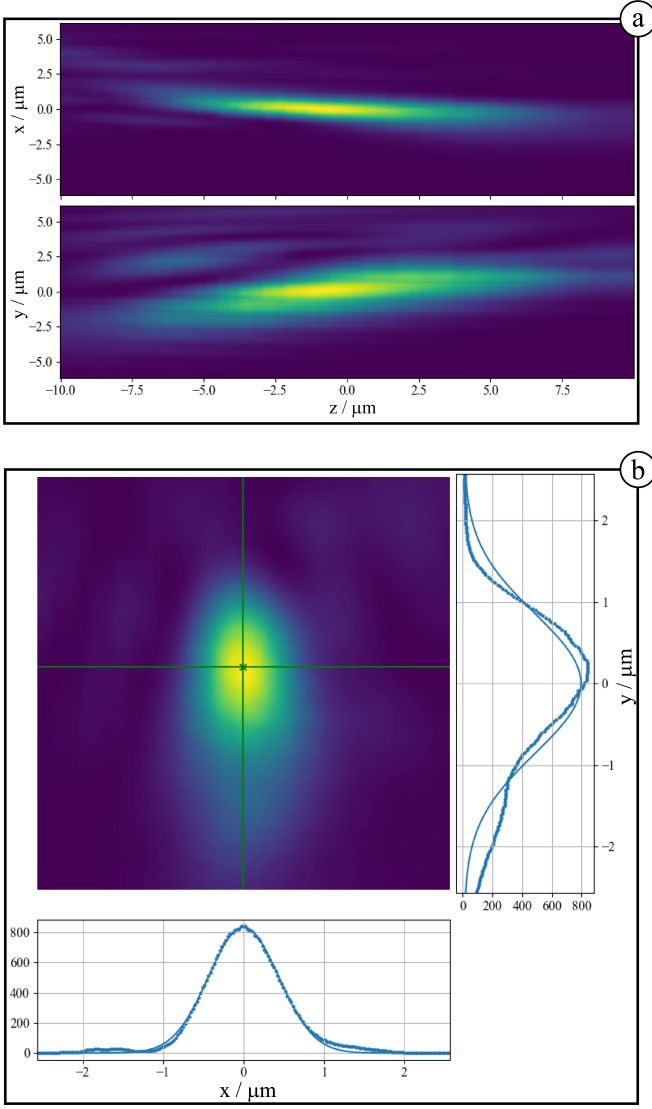


FIG. 5. (a): Beam profile of one of the optical channels of the integrated addressing unit showing the light propagation in x- and y-direction around the focal spot. (b): 2D plot of the focal spot at the ion location and 1D slices in x- and y-direction with Gaussian fit functions. The mode field diameter (MFD) in x- and y-direction at the focal spot is determined with $\text{MFD}_x = (1.73 \pm 0.01) \mu\text{m}$ and $\text{MFD}_y = (3.42 \pm 0.02) \mu\text{m}$, respectively.

ing, based on monolithic integration of the optical and electrical components, to a SiP approach. We have presented how in a SiP, different functional elements of the processor are realized on multiple chiplets that are optically and electrically interconnected. We have further discussed the technological advantages of the SiP approach. In particular, we discussed how it combines well-established processes for optical and electrical elements with fewer adaptations. The SiP approach also allows for greater flexibility in material selection and opens the door to novel functional elements that are difficult to realize with monolithic integration. Compared to monolithic in-

tegration, the SiP approach reduces the fabrication complexity of the individual chiplets, at the price of added complexity in the packaging of the SiP. The SiP approach makes design iterations and development of new functionalities faster and more cost-efficient, once the chiplet interfacing is established and remains unchanged.

We have described a proof-of-concept realization of a chiplet-based TIQC processor, which incorporates an integrated laser-addressing building block suited for individual ion addressing of ten ions in a linear crystal at a wavelength of 729 nm. The fabricated chiplet stack for this processor consists of the trap and PIC chiplet which are interfaced via Au-metal bonding. The trap chiplet is realized on a borosilicate glass substrate and carries aluminum filled TGVs for electrical interconnecting front metalization with the trap chiplet back side and PIC chiplet front side metalization used for signal fan-out. The PIC chiplet is equipped with optical waveguides and TIR mirrors for laser routing and out-coupling realized on a silicon substrate material. For individual ion addressing, a 3D-printed lens stack for imaging a waveguide array onto the ion positions is fabricated in a trench of the trap chiplet. The optical characterization of the addressing building block showed diffraction-limited spot sizes of about $1.7 \mu\text{m}$ in the trap's axial direction at a focal length of about $169 \mu\text{m}$, consistent with simulations. We further demonstrated successful bonding of the trap chiplet to the PIC chiplet using a low-temperature thermo-compression bond with an Au bond interface of about $20 \mu\text{m}$ thickness, which mitigates stress from the thermal expansion mismatch of the two chiplets. The demonstrated wafer-to-wafer bonding process was performed with relatively high forces to compensate for an Au surface roughness of approximately (8-14) nm. We assume that a die-to-die version of the bonding process requires a further reduction in the roughness of the gold surface. A die-to-die bond would be beneficial due to the simplification of the packaging workflow where the PIC chip facets could be polished prior to the bonding using established procedures.

In the future, the integrated addressing building block can be supplemented by additional integrated optics to also provide laser beams for ionization, laser cooling, and state readout. For these beams, individual ion addressing is typically not required such that the printed lens stack could be significantly simplified and its footprint reduced. The focusing unit could be further improved using an achromatic 3D printed lens stack, where polymers with different refractive index are being combined [76]. This could further reduce aberrations and allow one to use multiple addressing beams at different wavelengths to be focused by the same lens stack. 3D-printed polymer lenses will likely show problems for near-UV wavelengths, where currently employed polymers have high optical absorption and may even undergo bleaching. A hybrid approach, combining the established focusing grating couplers [22, 33] for global beams with the integrated addressing unit shown here, may thus be beneficial. The

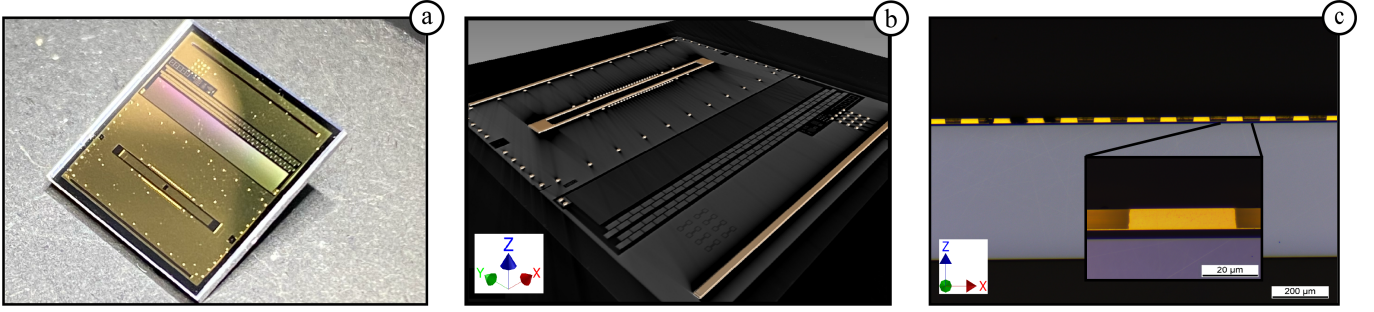


FIG. 6. (a): Image of a fabricated chiplet assembly. The trap chiplet metallization is a simplified design with only the bond structures required for this bond demonstration. (b): CT scan of the bond structures on top of the PIC chiplet metallization. (c): Micrograph image of several bonding interfaces with an enlarged micrograph image of a single bond structure.

beams emitted from grating couplers could also propagate through the transparent substrate material of the trap chiplet, removing the need for additional optical access slots.

Due to its inherent modular nature, chiplet integration is also ideal for incorporating additional technologies into large-scale TIQC processors. Integrated electronics such as digital-to-analog converters [38] or electrical switching electronics [43] could be realized on the PIC chiplet where the silicon substrate offers compatibility with established CMOS technologies. Similarly, passive components such as trench capacitors [27] for RF grounding of the trap’s DC control electrodes could be added. Other technologies may comprise active PIC elements to control laser phase, frequency, and amplitude [36], but also CMOS-compatible microheaters serving as a neutral atom source for ion loading [77]. The latter would require a loading slot in the trap chiplet, similar to the optical access slot shown in this work. Integrated photon detectors [34, 66] may likewise be added to the PIC chiplet. Here, one could even combine a 3D-printed focusing unit similar to the one shown in this work with a detector array to facilitate simultaneous state-readout of multiple ions in a crystal. Alternatively, the fluorescence light of individual ions in a chain could be coupled in an array of waveguides, each terminating at a detector, to further reduce readout crosstalk or allowing for photon-detection-mediated entangling operations [68, 78]. We stress that all these technologies do not need to be realized on a single chiplet. Multiple chiplets with different functional elements may be combined, e.g., laterally placed next to each other on a “supply layer” below the trap chiplet.

Finally, the SiP approach also offers a viable technological solution for the heterogeneous integration of optical components into segmented 3D ion traps produced by selective laser-induced etching (SLE) [79]. Since these traps typically employ glass substrates, one could possibly directly transfer the developed Au-metal bonding technology developed in this work to interface a segmented 3D ion trap to a PIC chiplet.

ACKNOWLEDGMENTS

The authors thank Dr. Simon Thiele of Printoptix GmbH for helpful discussions on two-photon polymerization technology and Dr. Renilkumar Mudachathi and Raimond Frentrop for their offered knowledge on the LioniX International BV waveguide technology. We would also like to thank Thomas Stöttinger and Marcus Dornetshumer of EV Group GmbH for sharing their knowledge in bonding technologies and for their willingness to work outside of standard specification guidelines. We gratefully acknowledge support by the European Union’s Horizon Europe research and innovation program under Grant Agreement Number 101114305 (“MILLENION-SGA1” EU Project), the European Union’s Horizon Europe research and innovation program under Grant Agreement Number 101046968 (BRISQ), the Austrian Science Fund (FWF Grant-DOI 10.55776/F71, 10.55776/COE1), the Austrian Research Promotion Agency (FFG) under the project “ScaleQubits” (914032), “SIQCI” (891364), “ITAQC” (896213), and “GLASTRAP” (915438), as well as the Intelligence Advanced Research Projects Activity (IARPA) and the Army Research Office, under the Entangled Logical Qubits program through Cooperative Agreement Number W911NF-23-2-0216.

AUTHOR CONTRIBUTIONS

B.B., P.H., T.M., and P.S. designed the experiment. B.B., M.R., and N.J. carried out the measurements and analyzed the data. B.B., P.H., H.Q., and D.K. fabricated the devices. B.B., P.H., and P.S. wrote the manuscript. All authors reviewed the manuscript. J.U., T.M., and P.S. supervised the project.

Appendix A: Additional bonding investigations

We verify the quality of the wafer-to-wafer Au-metal bond by performing CT measurements of the bond struc-

tures. We examine the bonding interfaces for open areas, in the Au-metal to ensure proper bonding quality, which compensates for the mechanical stress produced by the different thermal expansions of the trap and PIC chiplet substrate materials. This also ensures good electrical conductivity for routing the ion trap signals and seals the printed micro lens stack of the focusing unit during dicing. CT measurements in Fig. 8a and the acoustic microscopy investigations shown in Fig. 7 of an example sealing structure reveal an enclosed bonding surface throughout the observed interface. Additionally, no open metal areas were observed on the bonding pads surrounding the sealing structure. The cross sections in YZ-plane and XZ-plane in Fig. 8b,c confirm the successful bonding process.

In addition to the bonding quality, the wedge error between the trap and PIC chiplets was investigated. This is crucial for the function of the ion addressing building block, in which highly focused laser beams illuminate a linear ion crystal. If the crystal were not parallel to the PIC chiplet surface, it could not be guaranteed that the ions would see the smallest spot size. This would increase the optical crosstalk between several channels. We digitally measured the wedge error between both chiplets with cross sections of the chiplet stack in the XZ and YZ planes using CT scans. The error was determined to be $0.000^\circ \pm 0.002^\circ$.

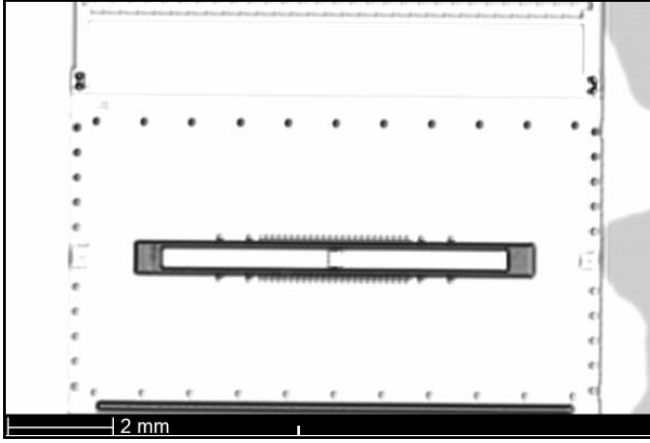


FIG. 7. Acoustic microscopy image of the sealing structure and the surrounding bonding pads. The dark areas indicate solid contact at the bonding surface. White areas represent open spaces. The absence of dark areas within the sealing structure indicates proper sealing function and the absence of water.

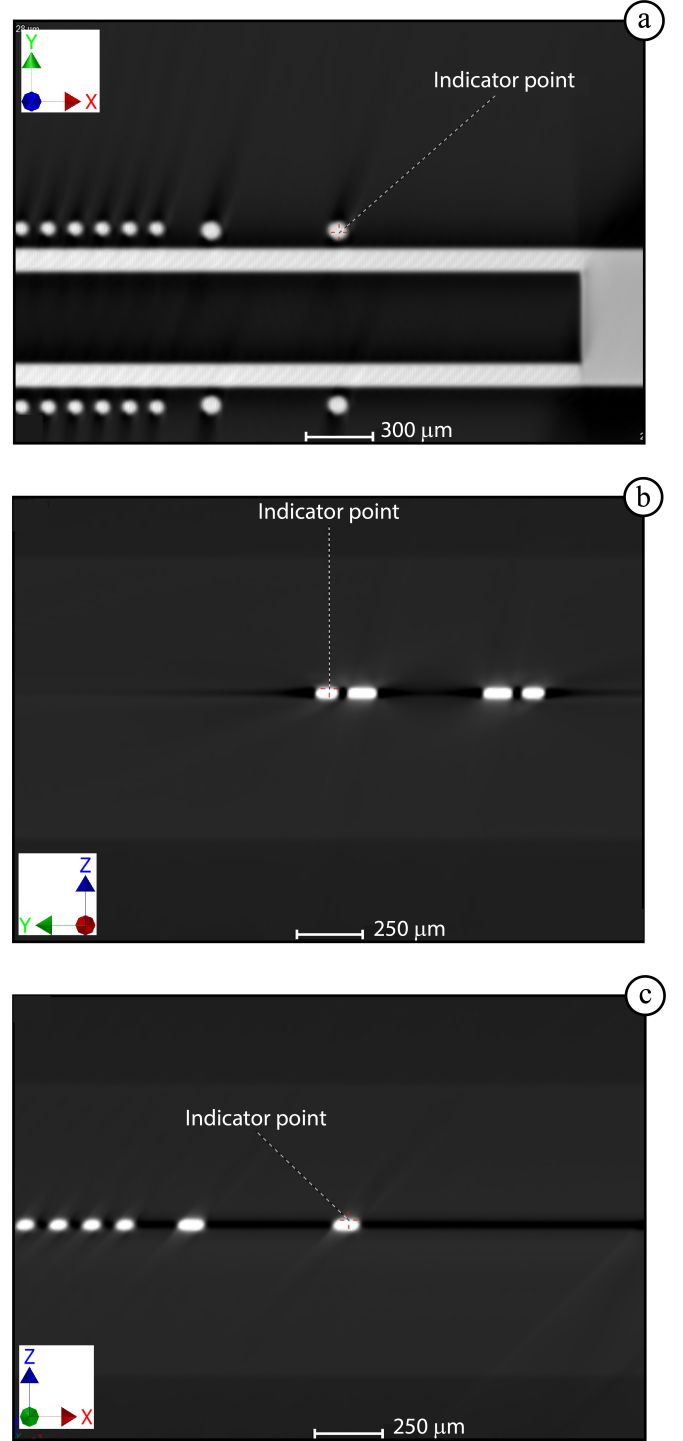


FIG. 8. (a): CT scan of the bonding interface with the rectangular sealing structure around the chiplet slot and multiple bonding pads (round) for electrical supply to the DC electrodes via the chiplet TGVs. White areas mark regions of high density (i.e. metal). (b): Cross section of the sealing and electrical bonding pads at the indicator point in the YZ-plane. (c): Cross section of the sealing and electrical bonding pads at the indicator point in the XZ-plane.

- [1] A. C. Hughes, R. Srinivas, C. M. Löschnauer, H. M. Knaack, R. Matt, C. J. Ballance, M. Malinowski, T. P. Harty, and R. T. Sutherland, Trapped-ion two-qubit gates with $>99.99\%$ fidelity without ground-state cooling (2025), [arXiv:2510.17286](#).
- [2] M. C. Smith, A. D. Leu, K. Miyanishi, M. F. Gely, and D. M. Lucas, Single-qubit gates with errors at the 10^{-7} level, *Phys. Rev. Lett.* **134**, 230601 (2025).
- [3] P. Wang, C.-Y. Luan, M. Qiao, M. Um, J. Zhang, Y. Wang, X. Yuan, M. Gu, J. Zhang, and K. Kim, Single ion qubit with estimated coherence time exceeding one hour, *Nat. Commun.* **12**, 233 (2021).
- [4] S. A. Moses, C. H. Baldwin, M. S. Allman, R. Ancona, L. Ascarrunz, C. Barnes, J. Bartolotta, B. Bjork, P. Blanchard, M. Bohn, J. G. Bohnet, N. C. Brown, N. Q. Burdick, W. C. Burton, S. L. Campbell, J. P. Campora, C. Carron, J. Chambers, J. W. Chan, and Y. H. e. a. Chen, A race-track trapped-ion quantum processor, *Phys. Rev. X* **13**, 10.1103/PhysRevX.13.041052 (2023).
- [5] L. Postler, S. Heußen, I. Pogorelov, M. Rispler, T. Feldker, M. Meth, C. D. Marciniak, R. Stricker, M. Ringbauer, R. Blatt, P. Schindler, M. Müller, and T. Monz, Demonstration of fault-tolerant universal quantum gate operations, *Nature* **605**, 675 (2022).
- [6] C. Ryan-Anderson, N. C. Brown, C. H. Baldwin, J. M. Dreiling, C. Foltz, J. P. Gaebler, T. M. Gatterman, N. Hewitt, C. Holliman, C. V. Horst, J. Johansen, D. Lucchetti, T. Mengle, M. Matheny, Y. Matsuoka, K. Mayer, M. Mills, S. A. Moses, B. Neyenhuis, and J. P. et. al, High-fidelity teleportation of a logical qubit using transversal gates and lattice surgery, *Science* **385**, 1327 (2024).
- [7] P. J. Ollitrault, M. Loipersberger, R. M. Parrish, A. Erhard, C. Maier, C. Sommer, J. Ulanis, T. Monz, C. Gogolin, C. S. Tautermann, G.-L. R. Anselmetti, M. Degroote, N. Moll, R. Santagati, and M. Streif, Estimation of electrostatic interaction energies on a trapped-ion quantum computer, *ACS Cent. Sci.* **10**, 882 (2024).
- [8] K. Seki, Y. Kikuchi, T. Hayata, and S. Yunoki, Simulating floquet scrambling circuits on trapped-ion quantum computers, *Phys. Rev. Res.* **7**, 023032 (2025).
- [9] Y. Zhu, Z. Zhang, B. Sundar, A. M. Green, C. Huerta Alderete, N. H. Nguyen, K. R. A. Hazzard, and N. M. Linke, Multi-round qaoa and advanced mixers on a trapped-ion quantum computer, *JQST* **8**, 015007 (2022).
- [10] D. Zhu, W. Shen, A. Giani, S. Ray-Majumder, B. Neculaes, and S. Johri, Copula-based risk aggregation with trapped ion quantum computers, *Sci. Rep.* **13**, 18511 (2023).
- [11] T. Proctor, K. Young, A. D. Baczewski, and R. Blume-Kohout, Benchmarking quantum computers, *Nature Rev. Phys.* **7**, 105 (2025).
- [12] D. Kielpinski, C. Monroe, and D. J. Wineland, Architecture for a large-scale ion-trap quantum computer, *Nature* **417**, 709 (2002).
- [13] R. B. Blakestad, C. Ospelkaus, A. P. VanDevender, J. M. Amini, J. Britton, D. Leibfried, and D. J. Wineland, High-fidelity transport of trapped-ion qubits through an x-junction trap array, *Phys. Rev. Lett.* **102**, 153002 (2009).
- [14] J. M. Pino, J. M. Dreiling, C. Figgatt, J. P. Gaebler, S. A. Moses, M. S. Allman, C. H. Baldwin, M. Foss-Feig, D. Hayes, K. Mayer, C. Ryan-anderson, and B. Neyenhuis, Demonstration of the trapped-ion quantum ccd computer architecture, *Nature* **592**, 209 (2021).
- [15] H. N. Tinkey, C. R. Clark, B. C. Sawyer, and K. R. Brown, Transport-enabled entangling gate for trapped ions, *Phys. Rev. Lett.* **128**, 050502 (2022).
- [16] M. Valentini, M. W. van Mourik, F. Butt, J. Wahl, M. Dietl, M. Pfeifer, F. Anmasser, Y. Colombe, C. Rössler, P. C. Holz, R. Blatt, A. Bermudez, M. Müller, T. Monz, and P. Schindler, Demonstration of two-dimensional connectivity for a scalable error-corrected ion-trap quantum processor architecture, *Phys. Rev. X* **15**, 041023 (2025).
- [17] Z. D. Romaszko, S. Hong, M. Siegle, R. K. Puddy, F. R. Lebrun-Gallagher, S. Weidt, and W. K. Hensinger, Engineering of microfabricated ion traps and integration of advanced on-chip features, *Nature Rev. Phys.* **2**, 278 (2020).
- [18] K. R. Brown, J. Chiaverini, J. M. Sage, and H. Häffner, Materials challenges for trapped-ion quantum computers, *Nature Rev. Mat.* **6**, 892 (2021).
- [19] M. G. Blain, R. Haltli, P. Maunz, C. D. Nordquist, M. Revelle, and D. Stick, Hybrid mems-cmos ion traps for nisc computing, *JQST* **6**, 034011 (2021).
- [20] S. Auchter, C. Axline, C. Decaroli, M. Valentini, L. Purwin, R. Oswald, R. Matt, E. Aschauer, Y. Colombe, P. Holz, T. Monz, R. Blatt, P. Schindler, C. Rössler, and J. Home, Industrially microfabricated ion trap with 1 ev trap depth, *JQST* **7**, 035015 (2022).
- [21] B. Lekitsch, S. Weidt, A. G. Fowler, K. Mølmer, S. J. Devitt, C. Wunderlich, and W. K. Hensinger, Blueprint for a microwave trapped ion quantum computer, *Sci. Adv.* **3**, e1601540 (2017).
- [22] R. J. Niffenegger, J. Stuart, C. Sorace-Agaskar, D. Kharas, S. Bramhavar, C. D. Bruzewicz, W. Loh, R. T. Maxson, R. McConnell, D. Reens, G. N. West, J. M. Sage, and J. Chiaverini, Integrated multi-wavelength control of an ion qubit, *Nature* **586**, 538 (2020).
- [23] K. K. Mehta, C. Zhang, M. Malinowski, T.-L. Nguyen, M. Stadler, and J. P. Home, Integrated optical multi-ion quantum logic, *Nature* **586**, 533 (2020).
- [24] J. Kwon, W. J. Setzer, M. Gehl, N. Karl, J. van der Wall, R. Law, M. G. Blain, D. Stick, and H. J. McGuinness, Multi-site integrated optical addressing of trapped ions, *Nat. Commun.* **15**, 3709 (2024).
- [25] D.-I. D. Cho, S. Hong, M. Lee, and T. Kim, A review of silicon microfabricated ion traps for quantum information processing, *MNSL* **3**, 10.1186/s40486-015-0013-3 (2015).
- [26] P. C. Holz, S. Auchter, G. Stocker, M. Valentini, K. Lakhmanskiy, C. Rössler, P. Stampfer, S. Sgouridis, E. Aschauer, Y. Colombe, and R. Blatt, 2d linear trap array for quantum information processing, *Advanced Quantum Technologies* **3**, 10.1002/qute.202000031 (2020).
- [27] J. D. Sterk, M. G. Blain, M. Delaney, R. Haltli, E. Heller, A. L. Holterhoff, T. Jennings, N. Jimenez, A. Kozhanov, Z. Meinelt, E. Ou, J. V. D. Wall, C. Noel, and D. Stick, Multi-junction surface ion trap for quantum computing (2024), [arXiv:2403.00208](#).
- [28] M. Dietl, M. Valentini, F. Anmasser, A. Zesar,

- S. Auchter, M. van Mourik, T. Monz, R. Blatt, C. Rössler, and P. Schindler, Test and characterization of multilayer ion traps on fused silica, *Advanced Quantum Technologies* **8**, [10.1002/qute.202500412](#) (2025).
- [29] C. D. Bruzewicz, J. M. Sage, and J. Chiaverini, Measurement of ion motional heating rates over a range of trap frequencies and temperatures, *Phys. Rev. A* **91**, [10.1103/PhysRevA.91.041402](#) (2015).
- [30] D. A. Hite, Y. Colombe, A. C. Wilson, K. R. Brown, U. Warring, R. Jördens, J. D. Jost, K. S. McKay, D. P. Pappas, D. Leibfried, and D. J. Wineland, 100-fold reduction of electric-field noise in an ion trap cleaned with in situ argon-ion-beam bombardment, *Phys. Rev. Lett.* **109**, 103001 (2012).
- [31] N. Daniilidis, S. Gerber, G. Bolloten, M. Ramm, A. Ransford, E. Ulin-Avila, I. Talukdar, and H. Häffner, Surface noise analysis using a single-ion sensor, *Phys. Rev. B* **89**, [10.1103/PhysRevB.89.245435](#) (2014).
- [32] P. Ramm, J. J.-Q. Lu, and M. M. V. Taklo, *Handbook of wafer bonding* (Wiley-VCH-Verl., Weinheim, 2012).
- [33] K. K. Mehta, C. D. Bruzewicz, R. McConnell, R. J. Ram, J. M. Sage, and J. Chiaverini, Integrated optical addressing of an ion qubit, *Nat. Nanotechnol.* **11**, 1066 (2016).
- [34] S. L. Todaro, V. B. Verma, K. C. McCormick, D. T. C. Allcock, R. P. Mirin, D. J. Wineland, S. W. Nam, A. C. Wilson, D. Leibfried, and D. H. Slichter, State readout of a trapped ion qubit using a trap-integrated superconducting photon detector, *Phys. Rev. Lett.* **126**, 010501 (2021).
- [35] W. J. Setzer, M. Ivory, O. Slobodyan, J. W. Van Der Wall, L. P. Parazzoli, D. Stick, M. Gehl, M. G. Blain, R. R. Kay, and H. J. McGuinness, Fluorescence detection of a trapped ion with a monolithically integrated single-photon-counting avalanche diode, *Appl. Phys. Lett.* **119**, 154002 (2021).
- [36] C. W. Hogle, D. Dominguez, M. Dong, A. Leenheer, H. J. McGuinness, B. P. Ruzic, M. Eichenfield, and D. Stick, High-fidelity trapped-ion qubit operations with scalable photonic modulators, *npj Quantum Information* **9**, [10.1038/s41534-023-00737-1](#) (2023).
- [37] M. Sieberer, C. Sandner, and P. Hadley, A cryogenic high-voltage amplifier for ion traps, in *SMACD / PRIME 2021* (2021) pp. 1–4.
- [38] J. Stuart, R. Panock, C. D. Bruzewicz, J. A. Sedlacek, R. McConnell, I. L. Chuang, J. M. Sage, and J. Chiaverini, Chip-integrated voltage sources for control of trapped ions, *Phys. Rev. Applied* **11**, 024010 (2019).
- [39] G. E. Moore, Cramming more components onto integrated circuits, reprinted from *electronics*, volume 38, number 8, april 19, 1965, pp.114 ff, *IEEE SSC-M* **11**, 33 (2006).
- [40] G. E. Moore, Progress in digital integrated electronics [technical literature, copyright 1975 ieee. reprinted, with permission. technical digest. international electron devices meeting, ieee, 1975, pp. 11-13.], *IEEE SSC-M* **11**, 36 (2006).
- [41] H. Wang, J. Ma, Y. Yang, M. Gong, and Q. Wang, A review of system-in-package technologies: Application and reliability of advanced packaging, *Micromachines* **14**, [10.3390/mi14061149](#) (2023).
- [42] M. Graef, More than moore white paper, in *2021 IEEE IRDS Outbriefs* (IEEE, 2021) pp. 1–47.
- [43] M. Malinowski, D. Allcock, and C. Ballance, How to wire a 1000-qubit trapped-ion quantum computer, *PRX Quantum* **4**, 040313 (2023).
- [44] P. Coudrain, J. Charbonnier, A. Garnier, P. Vivet, R. Vélard, A. Vinci, F. Ponthenier, A. Farcy, R. Segaud, P. Chausse, L. Arnaud, D. Lattard, E. Guthmuller, G. Romano, A. Gueugnot, F. Berger, J. Beltritti, T. Mourier, M. Gottardi, and S. e. a. Minoret, Active interposer technology for chiplet-based advanced 3d system architectures, in *2019 IEEE 69th ECTC* (2019) pp. 569–578.
- [45] D. Stick, W. K. Hensinger, S. Olmschenk, M. J. Madsen, K. Schwab, and C. Monroe, Ion trap in a semiconductor chip, *Nature Physics* **2**, 36 (2006).
- [46] H. Clauberg, A. Rezvani, V. Venkatesan, G. Frick, B. Chylak, and T. Strothmann, Chip-to-chip and chip-to-wafer thermocompression flip chip bonding, in *2016 IEEE 66th ECTC* (2016) pp. 600–605.
- [47] C.-K. Hsiung and K.-N. Chen, A review on hybrid bonding interconnection and its characterization, *IEEE Nanotechnol. Mag.* **18**, 41 (2024).
- [48] L. Sun, M. he Chen, L. Zhang, P. He, and L. sheng Xie, Recent progress in slid bonding in novel 3d-ic technologies, *J. Alloys Compd.* **818**, 152825 (2020).
- [49] B. Illés, A. Géczy, Z. Tafferner, A. Skwarek, and O. Krammer, Low-temperature soldering (lts) in the electronics industry: a brief review, in *2025 ISSE* (2025) pp. 1–6.
- [50] A. Khromova, C. Piltz, B. Scharfenberger, T. F. Gloger, M. Johanning, A. F. Varón, and C. Wunderlich, Designer spin pseudomolecule implemented with trapped ions in a magnetic gradient, *Phys. Rev. Lett.* **108**, 220502 (2012).
- [51] C. Monroe, R. Raussendorf, A. Ruthven, K. R. Brown, P. Maunz, L.-M. Duan, and J. Kim, Large-scale modular quantum-computer architecture with atomic memory and photonic interconnects, *Phys. Rev. A* **89**, 022317 (2014).
- [52] M. Akhtar, F. Bonus, F. R. Lebrun-Gallagher, N. I. Johnson, M. Siegle-Brown, S. Hong, S. J. Hile, S. A. Kulmiya, S. Weidt, and W. K. Hensinger, A high-fidelity quantum matter-link between ion-trap microchip modules, *Nat. Commun.* **14**, 531 (2023).
- [53] J. Chiaverini, R. B. Blakestad, J. Britton, J. D. Jost, C. Langer, D. Leibfried, R. Ozeri, and D. J. Wineland, Surface-electrode architecture for ion-trap quantum information processing, *Quantum Info. Comput.* **5**, 419–439 (2005).
- [54] K. Mehta, A. Ricci-Vasquez, C. Mordini, G. Beck, M. Malinowski, M. Stadler, C. Zhang, D. Kienzler, and J. Home, Ion trap quantum computing using integrated photonics, in *Integrated Optics: Devices, Materials, and Technologies XXVII*, Proceedings of SPIE, edited by S. M. García-Blanco and P. Cheben (SPIE, Bellingham, Washington, USA, 2023) p. 33.
- [55] T. Hu, X. Feng, Z. Yang, and M. Zhao, Design of scalable metalens array for optical addressing, *Front. Optoelectron.* **15**, 32 (2022).
- [56] M. Shirao, D. Klawson, S. Mouradian, and M. C. Wu, High efficiency focusing double-etched sin grating coupler for trapped ion qubit manipulation, *Jpn. J. Appl. Phys.* **61**, SK1002 (2022).
- [57] D. Chung, K. Choi, W. Lee, C. Kim, H. Shon, J. Park, B. Cho, K. Lee, S. Kim, S. Yoo, U. Jung, C. Jung, J. Kang, K. Kim, R. Berkis, T. Northup, D.-I. ‘Dan’ Cho, and T. Kim, A silicon-based ion trap chip protected from semiconductor charging, *JQST* **10**, 035014 (2025).

- [58] A. Bautista-Salvador, G. Zarantonello, H. Hahn, A. Preciado-Grijalva, J. Morgner, M. Wahnschaffe, and C. Ospelkaus, Multilayer ion trap technology for scalable quantum computing and quantum simulation, *New J. Phys.* **21**, 043011 (2019).
- [59] N. D. Guise, S. D. Fallek, K. E. Stevens, K. R. Brown, C. Volin, A. W. Harter, J. M. Amini, R. E. Higashi, S. T. Lu, H. M. Chanhvongsak, T. A. Nguyen, M. S. Marcus, T. R. Ohnstein, and D. W. Youngner, Ball-grid array architecture for microfabricated ion traps, *J. Appl. Phys.* **117**, 174901 (2015).
- [60] K. Wörhoff, R. G. Heideman, A. Leinse, and M. Hoekman, Triplex: a versatile dielectric photonic platform, *Adv. Opt. Technol.* **4**, 189 (2015).
- [61] Y. Su, Y. Zhang, C. Qiu, X. Guo, and L. Sun, Silicon photonic platform for passive waveguide devices: Materials, fabrication, and applications, *Adv. Mater. Technol.* **5**, 1901153 (2020).
- [62] H. Wang, T. C. Ralph, J. J. Renema, C.-Y. Lu, and J.-W. Pan, Scalable photonic quantum technologies, *Nature materials* **10.1038/s41563-025-02306-7** (2025).
- [63] S. Charles Doret, J. M. Amini, K. Wright, C. Volin, T. Killian, A. Ozakin, D. Denison, H. Hayden, C.-S. Pai, R. E. Slusher, and A. W. Harter, Controlling trapping potentials and stray electric fields in a microfabricated ion trap through design and compensation, *New J. Phys.* **14**, 073012 (2012).
- [64] E. Jansson, V. Scheuer, E. Jordan, K. Kostourou, and T. E. Mehlstäubler, Indium tin oxide combined with anti-reflective coatings with high transmittance for wavelengths ≥ 400 nm, *Appl. Opt.* **64**, 1715 (2025).
- [65] A. M. Eltony, S. X. Wang, G. M. Akselrod, P. F. Herskind, and I. L. Chuang, Transparent ion trap with integrated photodetector, *Appl. Phys. Lett.* **102**, 054106 (2013).
- [66] D. Reens, M. Collins, J. Ciampi, D. Kharas, B. F. Aull, K. Donlon, C. D. Bruzewicz, B. Felton, J. Stuart, R. J. Niffenegger, P. Rich, D. Braje, K. K. Ryu, J. Chiaverini, and R. McConnell, High-fidelity ion state detection using trap-integrated avalanche photodiodes, *Phys. Rev. Lett.* **129**, 100502 (2022).
- [67] B. Hampel, D. H. Slichter, D. Leibfried, R. P. Mirin, S. W. Nam, and V. B. Verma, Trap-integrated superconducting nanowire single-photon detectors with improved rf tolerance for trapped-ion qubit state readout, *Appl. Phys. Lett.* **122**, 10.1063/5.0145077 (2023).
- [68] F. W. Knollmann, S. M. Corsetti, E. R. Clements, R. Swint, A. D. Leu, M. E. Kim, P. T. Callahan, D. Kharas, T. Mahony, C. Sorace-Agaskar, R. McConnell, C. D. Bruzewicz, I. L. Chuang, J. Notaros, and J. Chiaverini, Collection of fluorescence from an ion using trap-integrated photonics (2025), [arXiv:2505.01412](https://arxiv.org/abs/2505.01412).
- [69] I. Charaev, D. A. Bandurin, A. T. Bollinger, I. Y. Phinney, I. Drozdov, M. Colangelo, B. A. Butters, T. Taniguchi, K. Watanabe, X. He, O. Medeiros, I. Božović, P. Jarillo-Herrero, and K. K. Berggren, Single-photon detection using high-temperature superconductors, *Nat. Nanotechnol.* **18**, 343 (2023).
- [70] I. Charaev, E. K. Batson, S. Cherednichenko, K. Reidy, V. Drakinskiy, Y. Yu, S. Lara-Avila, J. D. Thomsen, M. Colangelo, F. Incalza, K. Ilin, A. Schilling, and K. K. Berggren, Single-photon detection using large-scale high-temperature mgb2 sensors at 20 k, *Nat. Commun.* **15**, 3973 (2024).
- [71] I. Pogorelov, T. Feldker, C. D. Marciniak, L. Postler, G. Jacob, O. Krieglsteiner, V. Podlesnic, M. Meth, V. Negnevitsky, M. Stadler, B. Höfer, C. Wächter, K. Lakhmanskiy, R. Blatt, P. Schindler, and T. Monz, Compact ion-trap quantum computing demonstrator, *PRX Quantum* **2**, 020343 (2021).
- [72] A. Clark, Low temperature thermal expansion of some metallic alloys, *Cryogenics* **8**, 282 (1968).
- [73] D. James, Quantum dynamics of cold trapped ions with application to quantum computation, *Appl. Phys. B.* **66**, 181 (1998).
- [74] S. O'Halloran, A. Pandit, A. Heise, and A. Kellett, Two-photon polymerization: Fundamentals, materials, and chemical modification strategies, *Adv. Sci. (Weinh.)* **10**, e2204072 (2023).
- [75] M. Teller, D. A. Fioretto, P. C. Holz, P. Schindler, V. Messerer, K. Schüppert, Y. Zou, R. Blatt, J. Chiaverini, J. Sage, and T. E. Northup, Heating of a trapped ion induced by dielectric materials, *Phys. Rev. Lett.* **126**, 230505 (2021).
- [76] M. Schmid, F. Sterl, S. Thiele, A. Herkommer, and H. Giessen, 3d printed hybrid refractive/diffractive achromat and apochromat for the visible wavelength range, *Opt. Lett.* **46**, 2485 (2021).
- [77] V. Kumar, M. Siegle-Brown, P. Rahimi, M. Aylett, S. Weidt, and W. K. Hensinger, Fast-response low power atomic oven for integration into an ion microchip (2025), [arXiv:2503.10550](https://arxiv.org/abs/2503.10550).
- [78] F. W. Knollmann, E. Clements, P. T. Callahan, M. Gehl, J. D. Hunker, T. Mahony, R. McConnell, R. Swint, C. Sorace-Agaskar, I. L. Chuang, J. Chiaverini, and D. Stick, Integrated photonic structures for photon-mediated entanglement of trapped ions, *Optica Quantum* **2**, 230 (2024).
- [79] S. J. Simeth, A. Müller, J. Müller, B. Lekitsch, M. Reininghaus, and F. Schmidt-Kaler, Selective laser-induced etching for 3D ion traps, in *Laser-based Micro- and Nanoprocessing XVII*, Vol. 12409, edited by R. Kling, A. Watanabe, and W. Pfleging, International Society for Optics and Photonics (SPIE, 2023) p. 1240902.