

All-nitride superconducting qubits based on atomic layer deposition

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The development of large-scale quantum processors benefits from superconducting qubits that can operate at elevated temperatures and be fabricated with scalable, foundry-compatible processes. Atomic layer deposition (ALD) is increasingly being adopted as an industrial standard for thin-film growth, particularly in applications requiring precise control over layer thickness and composition. Here, we report superconducting qubits based on NbN/AlN/NbN trilayers deposited entirely by ALD. By varying the number of ALD cycles used to form the AlN barrier, we achieve Josephson tunneling through barriers of different thicknesses, with critical current density spanning seven orders of magnitude, demonstrating the uniformity and versatility of the process. Owing to the high critical temperature of NbN, transmon qubits based on these all-nitride trilayers exhibit microsecond-scale relaxation times, even at temperatures above 300 mK. These results establish ALD as a viable low-temperature deposition technique for superconducting quantum circuits and position all-nitride ALD qubits as a promising platform for operation at elevated temperatures.

INTRODUCTION

Superconducting qubits based on Josephson junctions have emerged as a leading platform for scalable quantum computing over the past few decades [1–4]. Among these, aluminum (Al)-based junctions are the most established, recently achieving wafer-scale fabrication suitable for large-scale processors [5]. However, such qubits typically operate below 100 mK. As the number of qubits increases, the cumulative heat load from qubit manipulation imposes stringent demands on cooling power. Raising cryostat temperatures is an efficient way to increase cooling power, motivating the development of qubits that can operate at higher temperatures [6–8].

Superconductors with higher critical temperatures (T_c) offer a path toward elevated-temperature operation. For instance, niobium (Nb)/Al/AlO_x qubits have demonstrated remarkable performance at elevated temperatures compared to pure Al due to the proximity effect [9–11]. Epitaxial NbN/AlN/NbN trilayer qubits, fabricated via dc-magnetron sputtering, have also emerged as a promising candidate by leveraging the even higher T_c of NbN and the potentially low-defect, crystalline AlN tunnel barriers [12, 13]. However, precise control of AlN thickness below 2 nm remains a key challenge, as small deviations can cause exponential variations in Josephson energy [14]. Additionally, the quality of the sputtered films is sensitive to substrate and buffer conditions, limiting reproducibility across wafers [15–17].

Atomic layer deposition (ALD) offers a compelling alternative for fabricating nitride-based superconducting circuits, particularly for its angstrom-level thickness con-

trol, excellent uniformity, and broad substrate compatibility [18, 19]. ALD is already integrated into advanced semiconductor manufacturing, enabling conformal coatings of high- κ dielectrics in transistor structures and memory cells, seed layers for interconnects, and pin-hole-free encapsulations [20–23]. Its scalability and CMOS compatibility make it a natural candidate for extending into superconducting quantum technologies. In recent years, ALD has been used to deposit high-quality NbN films with T_c around 13 K [24, 25], and Al₂O₃ tunnel barriers for Josephson junctions [26, 27]. However, to date, no superconducting qubits have been demonstrated based on ALD-grown trilayer materials.

In this work, we present the realization of NbN/AlN/NbN superconducting qubits using plasma-enhanced atomic layer deposition (PEALD). These all-nitride qubits are fabricated by a flip-chip bonding technique, which eliminates the use of lossy SiO₂ spacers while enabling independent optimization of the junction layers [9, 13, 28]. Importantly, the layer thickness can be precisely controlled at the atomic scale by adjusting the number of ALD cycles. DC transport measurements across wafers with varying AlN barrier thicknesses show that the critical current density (J_c) can be tuned over seven orders of magnitude, demonstrating the scalability and reproducibility of the ALD process. Transmon qubits fabricated from these trilayers exhibit microsecond-scale relaxation times, even when measured at temperatures above 300 mK. These results establish ALD-grown nitride trilayers as a promising material platform for scalable superconducting qubits with potential for elevated-temperature operation.

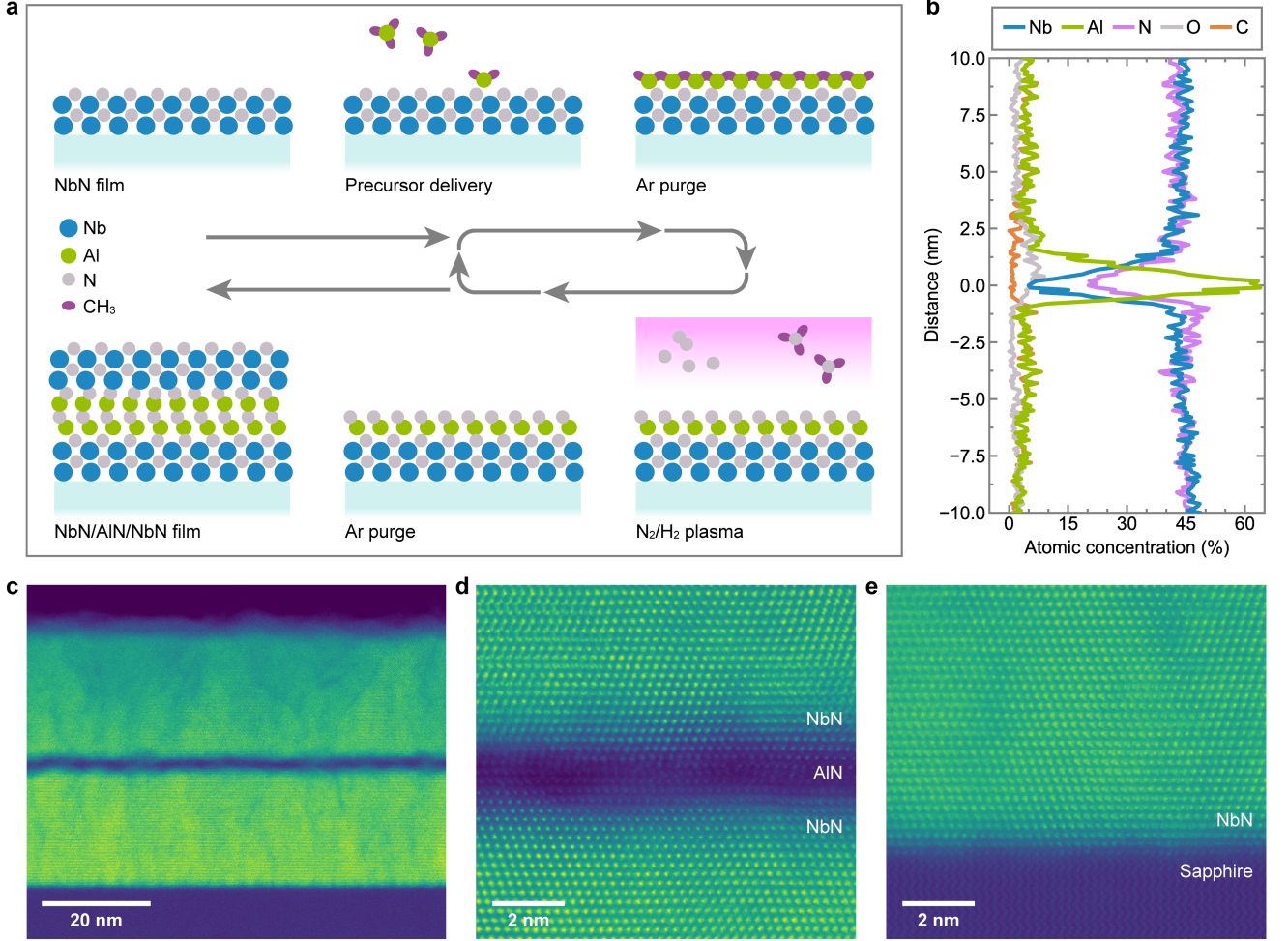


FIG. 1. **ALD growth sequence and atomic-scale characterization of NbN/AlN/NbN trilayer.** **a**, ALD process flow for trilayer deposition, following the arrows. NbN is first deposited on a c-plane sapphire substrate using the precursor TBTDEN. The Al-containing precursor (TMA) is then introduced and purged, followed by plasma-enhanced nitridation that converts surface-adsorbed Al into AlN. Residual ions and byproducts are subsequently removed in a second purge. Repeated cycles form the AlN barrier and NbN top layer, completing the NbN/AlN/NbN trilayer stack. **b**, 1D atomic concentration profile extracted from APT of a 15 nm-diameter cylindrical volume. The y-axis origin (0 nm) corresponds to the center of the AlN barrier; negative and positive distances denote the bottom and top NbN layers, respectively. **c**, Overview cross-sectional STEM image. **d**, Zoom-in STEM image of NbN/AlN/NbN interfaces. **e**, Magnified STEM image of NbN/sapphire interface.

RESULTS

ALD growth of NbN/AlN/NbN films and materials characterization

NbN/AlN/NbN trilayers are deposited on c-plane sapphire substrates using a remote plasma ALD system at temperatures ranging from 300 °C to 400 °C. Here, sapphire is used for its optical transparency, which facilitates flip-chip alignment. Similar trilayer growth is also achievable on silicon, supporting future CMOS-compatible integration with improved alignment strategies. As illustrated in the process schematic (Fig. 1a), layer-by-layer deposition of the nitride stack is achieved via alternating ALD cycles [24, 29, 30]. Each cycle begins with

the introduction of metal precursors (TBTDEN for NbN and TMA for AlN), carried by argon (Ar), followed by an Ar purge to ensure uniform adsorption on the substrate surface. A subsequent plasma step using a nitrogen/hydrogen (N₂/H₂) mixture initiates metal nitridation, after which a second Ar purge removes residual ions and byproducts. This cycle repeats until the desired thickness is achieved, forming a NbN/AlN/NbN trilayer. This self-limiting surface chemistry highlights ALD's capability of precise thickness control. To promote interface clarity and minimize residual contamination, additional ten cycles of plasma treatment are applied at the NbN/AlN interfaces.

To assess the structural quality of the nitride trilay-

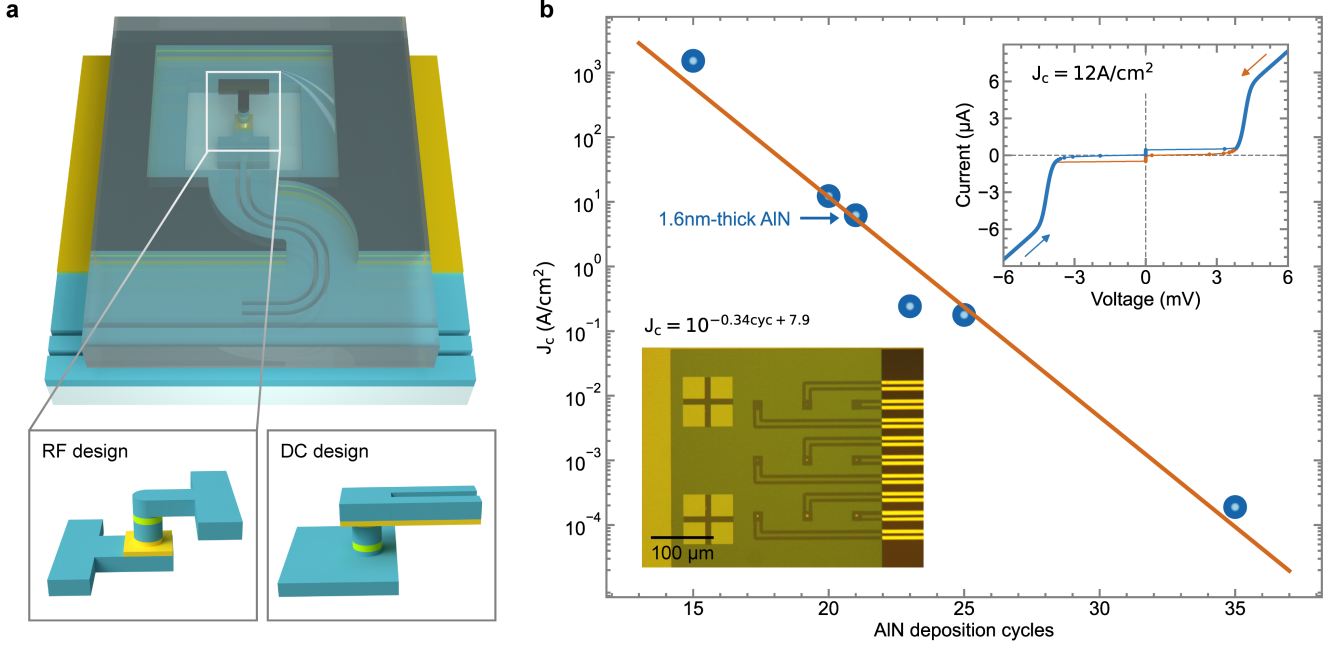


FIG. 2. Device schematics and IV characterization at 4K. **a**, A flip-chip qubit model, where the C-chip, consisting of a readout resonator and a transmission line, is at the bottom, while the Q-chip, hosting a junction, is on top. Blue, green, and yellow represent NbN, AlN, and gold, respectively. The lower-left panel shows a zoom-in model of the junction area, where two shunting pads ensure strong coupling of a qubit to the readout resonator. The lower-right panel shows a close-up view of a device used for DC characterization, in which the unetched bottom NbN film serves as the ground plane and the junction top electrode is flip-chip bonded to NbN-gold wires for readout. **b**, Dependence of J_c on the number of AlN deposition cycles. Blue dots represent experimental data from wafers grown over a year, while the orange curve is an exponential fit. The arrow indicates that 21 ALD cycles deposit ~ 1.6 nm-thick AlN, as estimated by STEM. The inset microscopic image shows nine junctions with two alignment crosses for flip-chip bonding. The inset IV curves correspond to a junction with 7 μm diameter.

ers, cross-sectional scanning transmission electron microscopy (STEM) is performed. The wider field-of-view image in Fig. 1c shows a uniform trilayer with a ~ 1.6 nm AlN barrier. The high-magnification image (Fig. 1e) reveals cubic-phase NbN deposited on the c-plane sapphire substrate, consistent with previous reports [31, 32]. The NbN layers consist of ~ 10 nm-wide twin domains oriented along the [111] direction, separated by vertical grain boundaries (Supplementary Section I). The atomic-resolution image of the NbN/AlN interfaces (Fig. 1d) reveals atomically sharp interfaces. Interestingly, the first few monolayers of AlN frequently exhibit features resembling the metastable cubic phase [33, 34], which then transitions into the thermodynamically favored hexagonal structure in subsequent layers [35]. While the detailed phase structure of AlN warrants further investigation, the well-defined trilayer geometry indicates its suitability for high-quality Josephson junctions. A ~ 2 nm amorphized NbO_x layer is also observed on the top surface of the layer stack, attributed to air exposure, but this thin oxide can be removed during subsequent device fabrication.

Atomic-scale chemical composition of the trilayers is further analyzed using atom probe tomography (APT).

A representative 1D concentration profile, extracted from a 15 nm-diameter cylinder cut across the layer stack, is shown in Fig. 1b. The Nb and Al profiles confirm the presence of a well-defined AlN barrier with minimal interdiffusion, while the N profile verifies successful nitridation across the interfaces. The elevated oxygen concentration ($\sim 5\%$) in the AlN layer, together with detectable carbon residues within all layers, suggests opportunities for further optimization of the growth process.

Josephson junction fabrication and DC transport characterization

The atomic-layer-deposited nitride trilayer offers a potentially high-quality AlN barrier with reduced oxygen content compared to the amorphous AlO_x barrier in Al-based qubits [13, 15]. However, forming Josephson junctions with this trilayer requires a more intricate fabrication process to establish a wiring layer that connects the top electrode while maintaining isolation from the bottom electrode. A conventional approach employs dielectric sidewall spacers for isolation [9, 12, 17, 36], but these can introduce additional microwave loss which degrades qubit coherence, and the added fabrication complexity

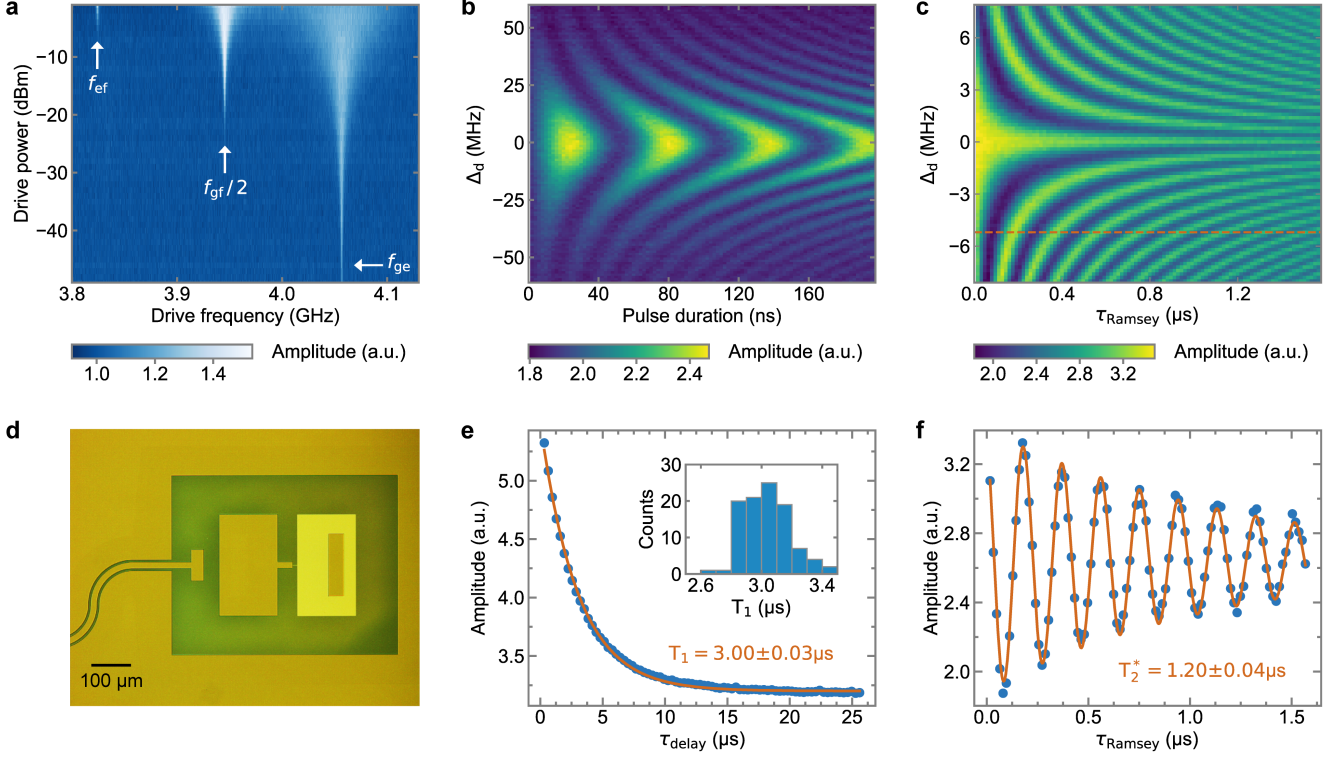


FIG. 3. **Qubit performance at the base temperature.** **a**, Power-dependent qubit spectroscopy. The power refers to the output level of a signal generator. The color bar represents the voltage amplitude of the transmitted probe tone. **b**, Chevron plot of Rabi oscillations. **c**, Ramsey oscillations measured near f_q with varying Δ_d . **d**, Microscopic image of a qubit and part of its readout resonator. **e**, T_1 characterization. The inset histogram summarizes the T_1 values from 100 repeated measurements taken over a two-hour period. The blue dots in the main graph represent averaged data from these repeated measurements. The orange curve is an exponential fit, yielding an average T_1 of $3.0 \mu\text{s}$. **f**, Extracted Ramsey oscillation from **c**, at $\Delta_d = -5.2 \text{ MHz}$. Orange curve is from a fitting model: $A_0 + Ae^{-\tau/T_2^*} \cos(2\pi\Delta_d\tau + \phi_0)$.

may create unintended lossy byproducts. To avoid dielectric spacers and simplify processing, we implement a flip-chip technique. Josephson junctions are patterned on the NbN/AlN/NbN trilayer chip (Q-chip), while a separate NbN single-layer chip (C-chip) defines the readout wiring. This modular fabrication approach offers greater flexibility, with the two chips interconnected via gold-gold bonding [37]. As illustrated in Fig. 2a, the 3D structure in the lower-right panel enables junction transport measurements through galvanic connections, while the other panels depict the flip-chip qubit realization with capacitive coupling to the environment (details in a later section).

The Josephson effect is characterized through DC current-voltage (IV) measurements at 4 K, using a typical device layout shown in the lower-left panel of Fig. 2b. As illustrated in the upper-right panel, the junctions display hysteretic behavior under bidirectional current sweeps. In the forward sweep (blue curve) with a positive current bias, a supercurrent flows up to the switching current (I_{sw}), beyond which Cooper pairs break, leading to a finite voltage readout. The observed I_{sw}

is lower than the theoretical critical current (I_c), likely due to environmental magnetic fields and residual RF noise. Above I_{sw} , quasiparticle-assisted tunneling dominates until the junction reaches the gap current (I_g), transitioning to the normal state. The reverse sweep (orange curve) retraces this behavior, with a return to the subgap regime as the current is reduced. We estimate I_c using an empirical relation $I_c = \pi I_g/4$, and determine the superconducting energy gap (2Δ) from the gap voltage (V_g), taken at a bias current $I_g/2$ [14, 15]. A key figure of merit for junction quality is the ratio of subgap resistance (R_{sg}) to normal-state resistance (R_n). The junction discussed here exhibits $R_{sg}/R_n = 47$ and $V_g = 4.2 \text{ mV}$. Across all measured wafers, the best device reaches $R_{sg}/R_n = 55$ and $V_g = 4.3 \text{ mV}$ (Supplementary Section IV), values that remain below but comparable to epitaxial NbN/AlN/NbN junctions [15, 17].

For a structurally uniform and pinhole-free tunnel barrier, the room-temperature conductance of Josephson junctions is expected to scale linearly with the junction area. This behavior is confirmed by our measurements (Supplementary Section IV), which reveal an inverse re-

relationship between resistance and area across an array of junctions on a single chip, indicating high lateral uniformity of the ALD-grown films. To further assess its ability of thickness control, we characterize chips from multiple wafers with varying AlN deposition cycles to extract J_c values at 4 K. As shown in Fig. 2b, J_c which spans a wide range from 10^{-4} to 10^3 A/cm² and decreases exponentially with increasing AlN cycles, following a relation $J_c \propto 10^{-0.34 \text{ cycle}}$. This strong correlation demonstrates that the AlN thickness increases linearly with ALD cycle number, even at the angstrom scale.

Qubit realization and characterization

Having established the Josephson tunneling characteristics of ALD-grown NbN/AlN/NbN trilayers, we next demonstrate transmon qubits based on this material platform. As illustrated in the flip-chip schematic (Fig. 2a) and the optical micrograph of a fabricated device (Fig. 3d), the Q-chip hosts junctions shunted by capacitive pads, while the C-chip contains the complementary pads and readout resonators. The Q-chips are fabricated from two wafers with J_c of 6 and 0.8 A/cm²; to-

gether with the variation in junction sizes, the resulting junction energy participation ratios (p_J) range from 0.2 to 0.8 (Supplementary Section V). Notably, qubits with the highest p_J resemble “*mergemons*”—a transmon variant [38, 39]—featuring micrometer-scale junctions and compact footprints, which are advantageous for large-scale quantum processors. The smallest junction diameter used in this study is 0.8 μm , demonstrating compatibility with photolithographic patterning and potential for integration with industrial fabrication workflows. To highlight its atomic layer deposition origin, we hereafter refer to this qubit structure as the *ALDmon*.

Similar to conventional transmons [40, 41], the *ALDmons* are designed with transition frequencies (f_q) of 4–5 GHz and are capacitively coupled to quarter-wave resonators operating in the 6–7 GHz range (f_c), with coupling strengths ($g/2\pi$) of approximately 50–70 MHz. Measurements are conducted in a dilution refrigerator at a base temperature of 10 mK. Qubit characterization begins with two-tone spectroscopy, where the transmission of a weak probe tone fixed at f_c is continuously monitored and a qubit drive tone is swept in power and frequency. As shown in Fig. 3a, at low drive power, the qubit transitions from ground to the first excited state (f_{ge} , denoted f_q in this study), observed as a change in the transmission amplitude of the probe tone. As the drive power increases, higher-energy transitions ($f_{gf}/2$ and f_{ef}) become resolvable and the anharmonicity ($\alpha/2\pi$) of 223 MHz can be extracted. The clean 2D spectroscopy map, free from spurious transitions, points out the high quality of the *ALDmon*’s tunnel barrier.

Based on the established qubit spectroscopy, we investigate qubit dynamics in the time domain [42, 43]. The detailed measurement setup is described in Supplementary Section III, where time-domain pulses at a drive frequency (f_d) and at f_c are used to excite the qubit and read out its state, respectively. As shown in Fig. 3b, at zero detuning, the qubit exhibits coherent oscillations between the ground $|g\rangle$ and the excited state $|e\rangle$ as the drive pulse duration increases, with a Rabi frequency Ω_R of 18 MHz. The brightest fringes on the 2D map correspond to the maximum $|e\rangle$ population. As detuning ($\Delta_d = f_d - f_q$) increases, the oscillation frequency rises to $\Omega = \sqrt{\Omega_R^2 + \Delta_d^2}$, while the excitation amplitude decreases. The resulting chevron pattern enables extracting the π -pulse duration at each detuning. Qubit relaxation time (T_1) is then measured by sweeping the delay (τ_{delay}) between the π -pulse excitation and the recording of the probe transmission, producing the result shown in Fig. 3e. A T_1 of $3.00 \pm 0.03 \mu\text{s}$ is obtained from 100 repeated measurements conducted over a two-hour period, with the statistical distribution displayed in the inset of Fig. 3e.

With the calibrated Rabi pulses, Ramsey measurements are performed to obtain the qubit coherence time (T_2^*). The qubit is first driven to the $(|g\rangle + |e\rangle)/\sqrt{2}$ state

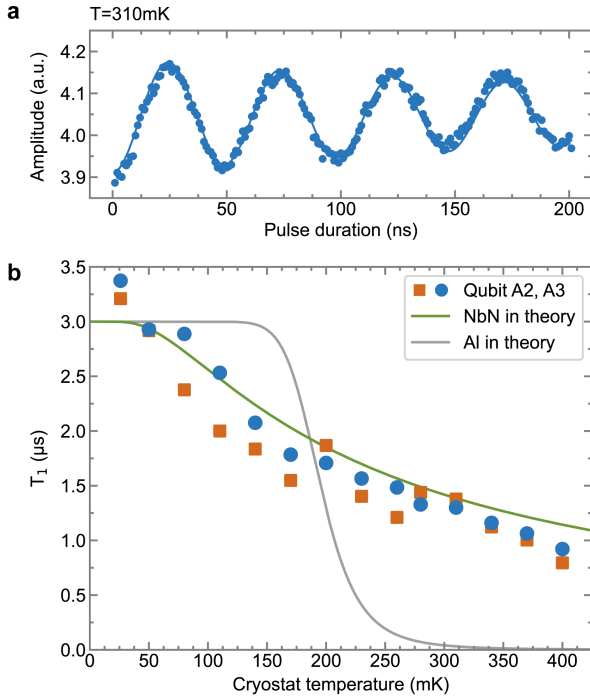


FIG. 4. **Qubit performance at elevated temperatures.** **a**, Rabi oscillation of qubit A3 as a function of pulse duration at 310 mK. **b**, orange squares and blue dots represent the T_1 values of qubits A2 and A3, respectively, across a temperature sweep. The green and gray curves show the theoretical temperature dependence of T_1 , as anticipated by the spin-boson model for NbN-based qubits and the quasiparticle relaxation model for Al-based qubits, respectively, both assuming $T_1 = 3 \mu\text{s}$ at 10 mK.

by a $\pi/2$ -pulse, then allowed to evolve freely for varying time intervals (τ_{Ramsey}), followed by a second $\pi/2$ -pulse and a final readout pulse. As shown in Fig. 3c, when $\Delta_d = 0$ MHz, the exponential decay of the readout amplitude reflects the loss of qubit coherence. When driven by a slightly detuned $\pi/2$ -pulse, the qubit accumulates a phase difference between $|g\rangle$ and $|e\rangle$ during its free evolution, leading to Ramsey oscillations in the time domain with frequency Δ_d . By fitting the exponential decay envelopes, we extract a T_2^* of $1.20 \pm 0.04 \mu\text{s}$, as shown in Fig. 3f, which is on the same order as T_1 .

A distinctive advantage of nitride superconductors is their high T_c , which makes it feasible to operate all-nitride qubits at elevated temperatures where Al-based qubits suffer from thermally excited quasiparticles [44–46]. To assess this capability, the performance of *ALDmons* in temperature regimes beyond the reach of conventional transmons is investigated. As a demonstration, a Rabi experiment is conducted at 310 mK on qubit A3 (previously discussed) and reveals well-resolved oscillations between $|g\rangle$ and $|e\rangle$ (Fig. 4a). This result confirms that NbN-based qubits can function at higher temperatures, despite the reduced signal to noise ratio caused by thermal photon population [47]. To further investigate temperature dependence, we conduct systematic T_1 measurements on qubits A2 (properties in Supplementary Section V) and A3 over a five-day temperature sweep from 400 mK down to 26 mK. At each temperature, qubits are allowed to thermalize for at least two hours prior to data acquisition. As shown in Fig. 4b, the measured gradual decrease of T_1 with temperature agrees well with the predictions from the spin-boson model, $T_1 \propto \left(1 + \coth\left(\frac{2\pi\hbar f_q}{2k_B T}\right)\right)^{-1}$ [48], indicated by the green curve. Crucially, unlike Al-based devices modeled by the gray curve in Fig. 4b, where T_1 exhibits a sharp drop beyond 200 mK [45, 49], our NbN/AlN/NbN *ALDmons* offer a significant operational advantage for future quantum technologies requiring relaxed thermal constraints.

DISCUSSION

In conclusion, we have demonstrated a new material platform for superconducting qubits based on atomic-layer-deposited NbN/AlN/NbN. Atomic-scale structural and compositional analyses confirm the uniformity and interface sharpness of the AlN tunnel barriers, while transport measurement highlights the precise thickness control inherent to the ALD process. The ability to span J_c over seven orders of magnitude validates the versatility of these trilayers for broad applications. In particular, qubits have been developed through integration with a flip-chip architecture. The *ALDmons* operate reliably not only at conventional millikelvin temperatures but also above 300 mK, expanding the temperature window for superconducting quantum devices.

Experimentally, *ALDmons* exhibit relaxation times in the range of 1–4 μs (Supplementary Section V), corresponding to quality factors ($Q_q = 2\pi f_q T_1$) of 0.4– 0.9×10^5 , motivating further investigation into potential loss mechanisms. As detailed in Supplementary Section VI, simulations indicate that the finite resistance of the gold bonding layer contributes a quality factor exceeding 3×10^6 , while the subgap conduction path through the AlN barrier corresponds to a Q above 5×10^5 . These estimations indicate that neither mechanism is the dominant source of loss in our current devices. Combined analysis and comparison with experimental data further confirm that the potential piezoelectricity of the AlN barrier does not limit the present Q_q . Although the predominant loss mechanisms in *ALDmon* remain unresolved, improvements in substrate quality, NbN dry etching, and device packaging are expected to further enhance qubit coherence [10, 50, 51].

With continued process optimization, *ALDmons*, potentially extending beyond the demonstrated NbN/AlN system to other nitride combinations, would be well-positioned to explore high-frequency operation in the millimeter wave regime and robust performance at elevated temperatures. These capabilities pave the way for a scalable and industry-compatible nitride-based platform for next-generation superconducting quantum technologies.

METHODS

The ALD process was carried out using a Ultratech/Cambridge Fiji G2 plasma system. Sapphire substrates were loaded into the chamber after sequential cleaning with organic solvents (NMP, acetone, and IPA), followed by a 10 min piranha treatment. Prior to deposition, the substrates underwent one cycle of N_2 and H_2 plasma surface activation. Tert-butylimido tris(diethylamido)niobium (TBTDEN) was the precursor for NbN deposition, while trimethylaluminum (TMA) served as the precursor for AlN. The plasma-enhanced deposition process utilized N_2 and H_2 as reactive gases. Across all wafers described in the main text, the two NbN layers in the trilayer structure maintained equal thickness, ranging from 25 nm to 50 nm.

A cross-section lamella for STEM was prepared using a Thermo Fisher Helios G4 UX Focused Ion Beam (FIB). Protective carbon and platinum layers were deposited on the lamella and prepared with a final milling step of 2 keV to reduce damage. STEM measurements were taken with an aberration-corrected Thermo Fisher Spectra 300 CFEG operated at 300 keV.

Needle-shaped APT specimens were prepared using a Thermo Fisher Helios 5UC dual-beam FIB/scanning electron microscope (SEM). The sharp APT needles were prepared by standard site-specific lift-out and annular milling methods. Special care was taken to capture all the layers of interest within the first 70 nm of the needle

without damaging the top layer. The APT data acquisition was performed on a CAMECA LEAP 5000XS instrument. The APT data analysis was conducted using CAMECA's Integrated Visualization and Analysis Software (IVAS 3.8). We note that nitrogen is systematically undercounted in the AlN barrier due to APT artifacts, arising from preferential field evaporation and the formation of neutral N₂ molecules in III-nitride semiconductors [52].

Detailed descriptions and figures on fabrication, measurement setups, and simulations, are provided in the Supplementary Sections.

Competing interests

The authors declare no competing interests.

Data availability

The data supporting this study are included in the article and its Supplementary Information. Further information are available from the corresponding authors on request.

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Contributions

H.X.T. and D.W. conceived the research and designed the experiments. D.W. deposited ALD films and fabricated devices with contributions from M.P. D.W. performed the DC measurement with contributions from C.B. Y.W. constructed RF measurement setup and

Y.W., D.W. performed the RF measurement. D.W., C.B. and M.P. provided the theoretical analysis. N.P. did STEM characterization. P.G. did APT characterization. H.X.T., D.M., B.M. supervised the project. D.W., N.P., P.G. and H.X.T. wrote the manuscript with input from all the authors.

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SUPPLEMENTARY INFORMATION

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I. FFT ANALYSIS OF STEM IMAGES

Fast Fourier transform (FFT) of the cross-sectional STEM image (Fig. 5a) is performed to examine the crystalline orientation across the NbN/AlN/NbN trilayer. As shown in Fig. 5b, the global FFT reveals twin domains, evidenced by two mirror-symmetric diffraction patterns along the $[111]$ direction. To further analyze these domains, multiple regions within the top and bottom NbN layers are selected for local FFTs. The FFT (Fig. 5c) from the red-marked regions in Fig. 5a shows grains oriented along the $[0\bar{1}1]$ direction, while the yellow-marked regions produce FFT patterns with orientation along the $[01\bar{1}]$ direction (Fig. 5d), confirming the presence of twin domains in the trilayer.

II. DEVICE FABRICATION

The overall flip-chip fabrication process involves two rounds of electron-beam lithography (EBL) on each chip. Notably, EBL is used based on the authors' preference; however, the process is fully compatible with photolithography, as the minimum feature size is approximately $0.8\ \mu\text{m}$. As illustrated in Fig. 6a, the first EBL is performed on the Q-chip to define the trilayer Josephson junctions and the gold bonding regions, using a bilayer resist stack composed of HSQ and PMMA for lift-off. After development, the Q-chip is transferred into an electron-beam evaporation system with ultra-high vacuum conditions ($< 10^{-8}$ Torr). The $\sim 2\ \text{nm}$ NbO_x is removed by Ar plasma milling, followed by *in situ* deposition of a 10 nm gold/50 nm titanium (Ti) bilayer without breaking vacuum. Ti serves as a hard mask for subsequent NbN etching and is later removed using hydrofluoric acid (HF). The top NbN layer and the underlying AlN layer are patterned using reactive ion etching (RIE) with a CF₄/Ar gas mixture; this recipe is consistently applied to all etching steps throughout the process. After being cleaned in acetone and IPA, the Q-chip undergoes the second EBL using PMMA as the resist (Fig. 6b). This step defines the removal of the bottom NbN layer everywhere except for the capacitive pads near the junctions. After solvent cleaning and an HF dip, the Q-chip is ready for bonding.

The C-chip fabrication process follows a similar but simplified procedure. As depicted in Fig. 6c, the 10 nm-thick gold bonding layer is deposited after EBL patterning and surface treatment. Subsequently, the readout resonators and other control circuits are defined via EBL and formed using the same RIE method (Fig. 6d). Similar to the Q-chip, C-chip is cleaned by organic solvents followed by an HF dip. Prior to bonding, both chips are exposed to a 30 s, 100 W Ar plasma treatment to activate the surface. Finally, flip-chip bonding is performed at room temperature using a Tresky T-3000 Pro, achieving alignment precision better than $5\ \mu\text{m}$.

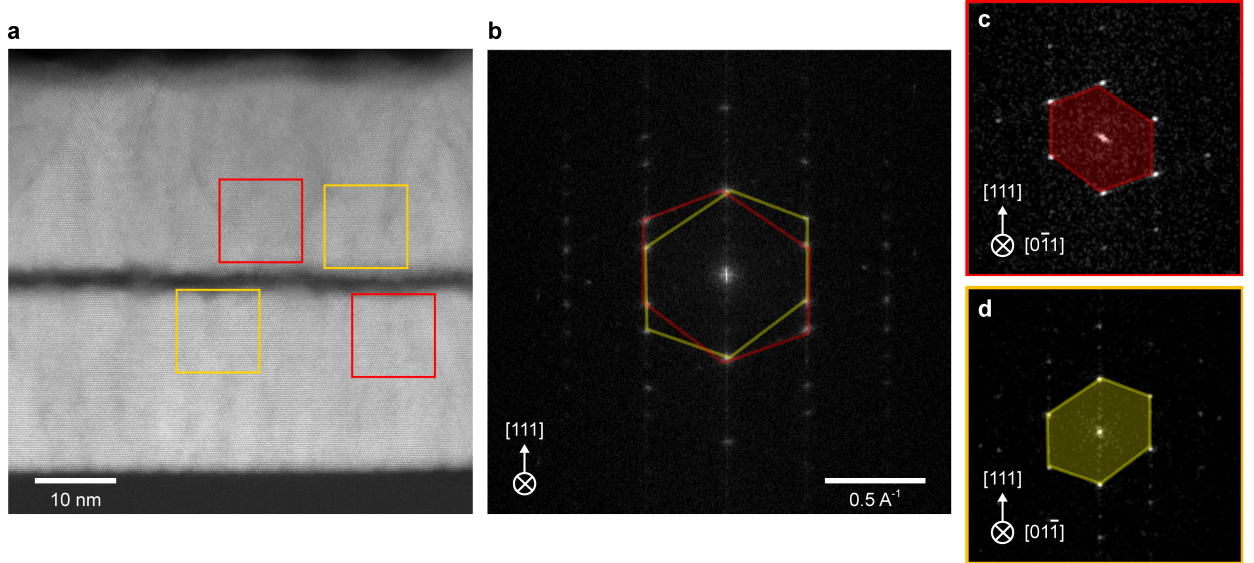


FIG. 5. **STEM image of NbN/AlN/NbN trilayer and corresponding FFTs.** **a**, Cross-sectional annular dark-field (ADF) STEM image of the trilayer. Regions outlined in red and yellow are selected for local FFT analyses. **b**, Global FFT of the entire field of view in **a**, indicating twin domains along the $[111]$ direction. **c**, FFT of red-marked regions in **a**, showing grains oriented along the $[0\bar{1}1]$ direction. **d**, FFT of yellow-marked regions in **a**, showing grains oriented along the $[01\bar{1}]$ direction. The shaded regions in **c,d** highlight the inner diffraction patterns that reflect mirror symmetry along the $[111]$ direction.

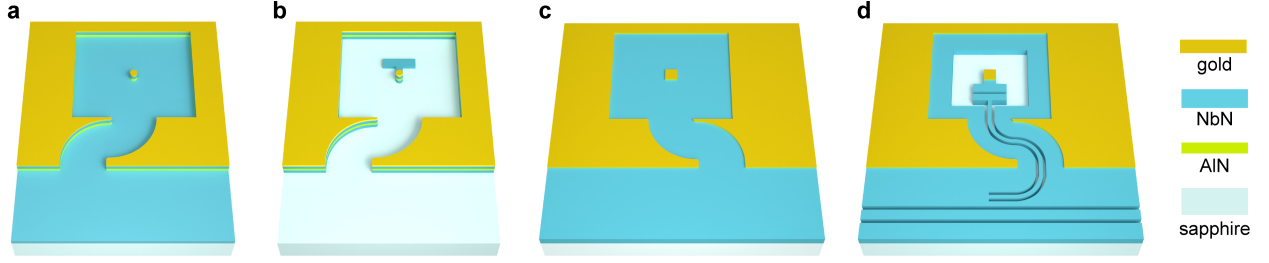


FIG. 6. **Schematics of the fabrication process.** **a**, Step1 of Q-chip: deposition of gold for bonding; RIE of the top NbN and the AlN barrier for junction formation. **b**, Step2 of Q-chip: RIE of the bottom NbN to define the shunting pads of qubits. **c**, Step1 of C-chip: deposition of gold for bonding. **d**, Step2 of C-chip: RIE of NbN to generate control circuits.

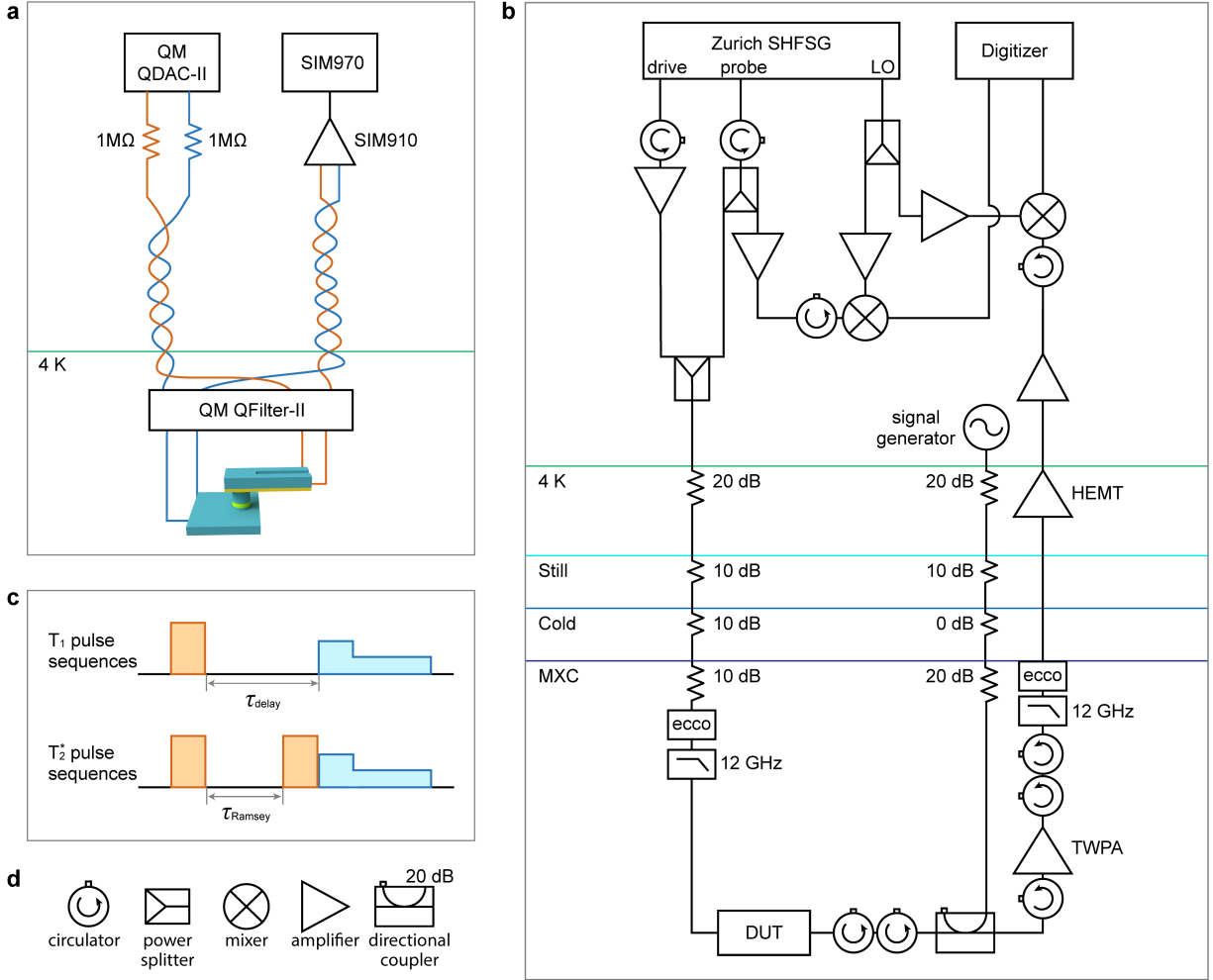


FIG. 7. **Measurement Setup.** **a**, Setup for IV characterization of junctions. **b**, Setup for qubit time-domain measurement. Unnamed components in the setup are labeled in **d**. **c**, Drive and probe pulse sequences for T_1 and T_2^* measurements.

III. MEASUREMENT SETUP

Devices used for IV characterization presented in Fig. 2 of the main text are mounted inside a 4 K cryostat. A QFilter-II from Quantum Machines (QM) is installed near the devices at the 4 K stage to suppress electromagnetic noise above 65 kHz. As illustrated in Fig. 7a, the device is current-biased using a voltage source (QDAC-II), with two 1 MΩ resistors in series to ensure stable current flow. The voltage drop across the device is amplified using a voltage

preamplifier (SIM910), and the amplified signal is subsequently recorded by a digital voltmeter (SIM970).

Devices used for qubit characterization, shown in Fig. 3 of the main text, are enclosed in a copper box for electromagnetic shielding and mounted in a Bluefors dilution refrigerator. Frequency-domain measurements, such as two-tone spectroscopy, are performed using a Zurich SHFLI lock-in amplifier, while the time-domain measurement setup is illustrated in Fig. 7b. A Zurich SHFSG signal generator is utilized to provide a qubit drive tone, a probe tone and a local oscillator (LO). The drive and probe tones are combined, attenuated by 50 dB at cryogenic stages, filtered by an Eccosorb infrared filter and a 12 GHz low-pass filter, and then sent to the device. The output signal is amplified by a traveling-wave parametric amplifier (TWPA) in the mixing chamber, a high-electron-mobility transistor (HEMT) at 4 K, and additional room-temperature amplifiers. It is then demodulated using the LO (75 MHz frequency offset from the probe tone) and recorded by a digitizer (ATS9373). A 75 MHz reference path, generated by mixing the LO and the probe tone directly from SHFSG, is used for phase correction.

Using the established setup, a qubit is excited by a rectangular π -pulse, and its T_1 is extracted by fitting the probe transmission amplitudes after a set of delay times (τ_{delay}). As shown by the blue envelope of the readout pulse in Fig. 7c, a short and strong pulse is first applied to the cavity to rapidly populate cavity photons, thereby improving the signal-to-noise ratio [1]. Similarly, in Ramsey experiments, probe amplitudes are recorded after applying two separated $\pi/2$ -pulses to the qubit, and T_2^* is obtained by fitting the exponentially decayed oscillations. During the elevated-temperature measurements (Fig. 4 of the main text), we employ extensive signal averaging to suppress noise related to the thermal excitation of qubit states: each pulse duration in the Rabi measurements is averaged 250,000 times, and each delay point in the T_1 measurements is averaged 600,000 times (50 delay points for T_1 extraction).

IV. JUNCTION DC CHARACTERIZATION

NbN/AlN/NbN trilayer junctions are systematically characterized at both room temperature (RT) and 4 K. To illustrate typical device performance, we present detailed characterization of a representative wafer below. As shown in Fig. 8a, the RT resistance (R) scales inversely with the junction area (A), following the relation $RA = \text{const.}$ This behavior confirms a uniform AlN barrier.

Fig. 8b shows the IV characteristic of a representative junction with a $2\ \mu\text{m}$ diameter measured at 4 K. Its superconducting energy gap (2Δ) is 4.3 meV, and J_c is approximately $6\ \text{A}/\text{cm}^2$. The normal-state resistance (R_n) is $14.6\ \text{k}\Omega$, calculated from the slope of the normal state region, while the subgap resistance (R_{sg}) reaches $0.80\ \text{M}\Omega$ at an applied voltage of 3 mV, as highlighted in the inset. This wafer exhibits the highest R_{sg}/R_n ratio among all wafers characterized, and is selected for qubit fabrication. The low switching current (I_{sw}) observed in the nanoampere range is likely affected by environmental magnetic fields and residual RF noise, which may be improved by better electromagnetic shielding.

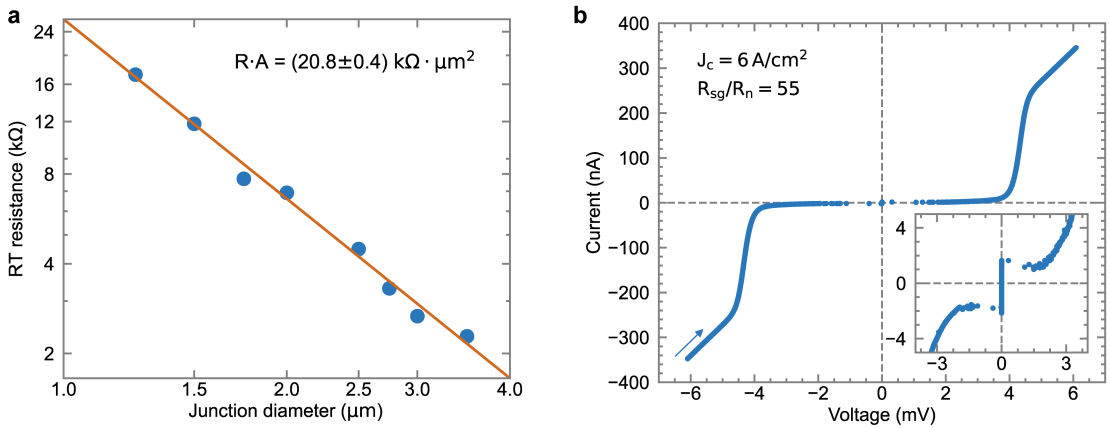


FIG. 8. **DC transport characterization of Josephson junctions.** **a**, RT resistance of junctions as a function of diameters. The orange line is a fit assuming constant resistance–area product, yielding a value of $20.8\ \text{k}\Omega \cdot \mu\text{m}^2$ with a standard error of $0.4\ \text{k}\Omega \cdot \mu\text{m}^2$. **b**, IV curve of a selected junction, where bias current is swept from negative to positive values. The inset shows a magnified view of the subgap region.

V. QUBIT DESIGN AND PERFORMANCE

The *ALDmon* circuit consists of a transmission line, multiple *ALDmons*, and their associated readout resonators. A distinguishing feature of our design is the flip-chip architecture, with shunting capacitive pads distributed across two separate chips, which simplifies fabrication but adds complexity to simulation. To model the flip-chip structure, electromagnetic simulations are performed using Sonnet, based on a geometry consisting of two substrates separated by a vacuum gap of several tens of nanometers. The resonant frequencies of *ALDmons* and readout cavities are simulated, incorporating the kinetic inductance of the NbN thin film (7 pH/square for a 50 nm-thick NbN layer). Furthermore, the coupling strength ($g/2\pi$) between an *ALDmon* and its readout resonator is extracted by intentionally bringing their resonances into degeneracy and analyzing the resulting mode splitting.

Two wafers, labeled A and B, with J_c of 6 A/cm² and 0.8 A/cm², respectively (estimated from IV characteristics), are processed to fabricate qubits with transition frequencies (f_q) in the range of 4–5 GHz. To characterize *ALDmons*' geometry, we introduce the junction energy participation ratio (p_J), defined as the fraction of electric field energy stored in the junction: $p_J = C_J/C_\Sigma$, where C_J is the junction capacitance and C_Σ is the total qubit capacitance. Conventional planar transmons, where large shunting capacitors dominate C_Σ , exhibit $p_J \sim 0.02$, whereas “*mergemons*” have $p_J \sim 0.9$, as most of their capacitance originates from the junction itself [2–4]. For wafer A, junctions with diameters of 1 μm and 0.8 μm are used, resulting in p_J ranging from 0.30 to 0.20—intermediate between transmons and mergemons. For wafer B, 2 μm junctions are employed to realize qubits approaching the mergemon regime. Experimental parameters of the five *ALDmons* are summarized in Tab. I.

VI. ANALYSIS OF LOSS CHANNELS

We analyze the potential loss channels of the *ALDmon* devices using a conventional energy participation model and provide promising strategies to further enhance qubit coherence [8, 9]. Contributions to the overall qubit quality factor (Q_q) can be decomposed into several independent loss channels: $\frac{1}{Q_q} = \frac{1}{Q_{JJ_subgap}} + \frac{1}{Q_{AlN_piezo}} + \frac{1}{Q_{Au}} + \frac{1}{Q_{other}}$. Here, $1/Q_{JJ_subgap}$ denotes dissipation from junction subgap conduction path, $1/Q_{AlN_piezo}$ is the potential piezoelectric loss from the AlN barrier, $1/Q_{Au}$ represents loss due to the gold layer, and $1/Q_{other}$ includes contributions from surface niobium oxide, the NbN-sapphire interface, crystalline defects in bulk sapphire, and device packaging. Given the unique aspects of our junction materials and the use of gold for flip-chip bonding, we focus our analysis on the first three channels and provide theoretical estimates of Q_{JJ_subgap} , Q_{AlN_piezo} and Q_{Au} .

Qubit	A1	A2	A3	B1	B2
f_q (GHz)	5.063	4.089	4.057	3.983	3.907
E_J (GHz)	20.020	11.790	11.545	11.980	11.189
E_C (GHz)	0.172	0.196	0.197	0.182	0.188
$g/2\pi$ (MHz)	48.7	67.5	68.5	49.0	55.0
δf_c (MHz)	2.04	1.53	1.45	1.40	1.31
f_c (GHz)	6.8855	6.9657	7.0874	5.8848	6.2171
$Q_{ci} (\times 10^3)$	44.5	25.1	56.4	45.3	36.6
T_1 (μs)	1.43 ± 0.03	2.87 ± 0.07	3.00 ± 0.03	2.66 ± 0.05	3.43 ± 0.08
T_2^* (μs)	0.74 ± 0.04	0.65 ± 0.04	1.20 ± 0.04	0.69 ± 0.04	NA
D_J (μm)	1	0.8	0.8	2	2
p_J	0.30	0.20	0.20	0.75	0.74

TABLE I. **Parameters of 5 qubits.** Here, f_q denotes the qubit transition frequency from the ground to the excited state. E_J and E_C are the Josephson and charging energies, respectively. $g/2\pi$ is the qubit–cavity coupling strength, and the parameters E_J , E_C and $g/2\pi$ are calculated using scqubits [5, 6]. δf_c represents the shift of the cavity frequency from its bare value due to the qubit coupling. f_c is the shifted cavity frequency; Q_{ci} is the single-photon-level intrinsic quality factor of the shifted cavity. T_1 and T_2^* are the qubit’s relaxation time and Ramsey coherence time, respectively. The error represents the standard error from fitting, consistent with those values in the main text. D_J is the junction diameter, and p_J is the junction energy participation ratio.

e_{33} (C/m ²)	e_{31} (C/m ²)	D_J (μm)	p_J	$Q_{\text{AlN,piezo}}$
1.41	-0.55	0.8	0.20	8.3×10^3
0.451	-0.176	0.8	0.20	8.1×10^4
0.141	-0.055	0.8	0.20	8.3×10^5
1.41	-0.55	2.0	0.75	1.9×10^3
0.451	-0.176	2.0	0.75	1.8×10^4
0.141	-0.055	2.0	0.75	1.9×10^5

TABLE II. **Simulated $Q_{\text{AlN,piezo}}$ for different AlN piezoelectric constants and qubit geometries.** The piezoelectric stress constants e_{33} and e_{31} of row 1 correspond to typical values for wurtzite AlN [7]. D_J is the diameter of Josephson junction in the simulations, and p_J is the junction energy participation ratio obtained from Tab. I.

The subgap conduction path through the AlN barrier is reflected in the finite R_{sg} . From transport data, a junction with I_c of 86 nA exhibits a R_{sg} of 260 MΩ at 10 mK under a 0.5 mV DC bias. Since *ALDmons* studied in this work have lower I_c and require much smaller voltage excitation, this measurement provides a conservative lower bound for $Q_{\text{JJ,subgap}}$, estimated as: $Q_{\text{JJ,subgap}} = \omega_q C_\Sigma R_{\text{sg}} \gtrsim 5.7 \times 10^5$, which is well above our measured qubit quality factors ($Q_q = \omega_q T_1$, ranging from 45×10^3 to 84×10^3 , with $\omega_q = 2\pi f_q$).

Piezoelectric loss can arise when superconducting circuits couple to materials or interfaces with intrinsic piezoelectricity [10, 11]. Wurtzite AlN is a well-established piezoelectric material capable of dissipating electromagnetic energy via electromechanical coupling. However, in our *ALDmon*, the coexistence of cubic and hexagonal phase AlN may weaken the piezoelectricity, and detailed analysis in the following prove that the piezoelectric loss is not the main bottleneck. Since the piezoelectric properties of our AlN film are uncertain, we consider a range of piezoelectric stress constants (e_{33} and e_{31}) from typical wurtzite AlN values to one order of magnitude lower. The simulations are performed in COMSOL, and $Q_{\text{AlN,piezo}} = \frac{\omega_q E_{\text{em}}}{p_J P_{\text{mech}}}$, where E_{em} is the stored electromagnetic energy in NbN/AlN/NbN junction and P_{mech}/ω_q is the dissipated mechanical energy per cycle. As summarized in Tab. II, $Q_{\text{AlN,piezo}}$ scales approximately as $1/e^2$, evident from rows 1–3, and also shows strong dependence on qubit geometry, as seen by comparing rows 1 and 4, corresponding to the geometry of qubits A3 and B1 (Tab. I). Experimentally, however, the similar Q_q values of A3 and B1 confirm that our AlN exhibits very low piezoelectricity, demonstrating that piezoelectric loss is not the dominant qubit loss channel.

Another innovation in our qubit design is the use of gold for flip-chip bonding, including gold on the ground plane for supporting and directly on the junctions for galvanic connection. We first characterized NbN resonators with gold deposited on the ground plane at 3 K and extracted an equivalent gold resistivity of $6 \times 10^{-11} \Omega \cdot \text{m}$. Based on this low resistive value, the supporting gold layer is deposited far away from qubits, to ensure a minor electric field distribution on the gold and negligible loss contribution. As for gold layers deposited directly above the junctions, experimental data show no clear correlation between T_1 and the gold footprint (Tab. I). Theoretically, we estimate the effect of series resistance from gold (R_{Au}) using a lumped-element model: $Q_{\text{Au}} \simeq \frac{1}{\omega_q C_\Sigma R_{\text{Au}}} \left(\frac{C_\Sigma}{C_\Sigma - C_J} \right)^2 \gtrsim 3.3 \times 10^6$, where a gold resistivity of $6 \times 10^{-9} \Omega \cdot \text{m}$ is assumed to provide a highly conservative lower bound for Q_{Au} . Together, these experimental and theoretical results confirm that the gold layer does not limit device performance.

Based on the above analysis, we conclude that the performance of the devices presented in this work is not limited by the AlN barrier nor the flip-chip bonding approach. The predominant loss mechanism remains under investigation. Future studies will focus on varying E_J and E_C of *ALDmons* to probe possible frequency dependence of T_1 . Meanwhile, we will pursue improvements through fabrication refinements, including the use of high-quality substrates with advanced surface treatments, minimizing fluorocarbon byproducts during the RIE process, and incorporating additional post-RIE cleaning steps on the NbN surface [12–14]. Looking ahead, we anticipate broader applications of *ALDmons* as coherence times continue to improve.

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