FPGA-Accelerated RISC-V ISA Extensions for Efficient Neural Network Inference on Edge Devices

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***Abstract*—Edge AI deployment faces critical challenges balancing computational performance, energy efficiency, and resource constraints. This paper presents FPGA-accelerated RISC-V instruction set architecture (ISA) extensions for efficient neural network inference on resource-constrained edge devices. We introduce a custom RISC-V core with four novel ISA extensions (FPGA.VCONV, FPGA.GEMM, FPGA.RELU, FPGA.CUSTOM) and integrated neural network accelerators, implemented and validated on the Xilinx PYNQ-Z2 platform.**

The complete system achieves 2.14× average latency speedup and 49.1% energy reduction versus an ARM Cortex-A9 software baseline across four benchmark models (MobileNet V2, ResNet-18, EfficientNet Lite, YOLO Tiny). Hardware implementation closes timing with +12.793 ns worst negative slack at 50 MHz while using 0.43% LUTs and 11.4% BRAM for the base core and 38.8% DSPs when accelerators are active. Hardware verification confirms successful FPGA deployment with verified 64 KB BRAM memory interface and AXI interconnect functionality.

All performance metrics are obtained from physical hardware measurements. This work establishes a reproducible framework for ISA-guided FPGA acceleration that complements fixed-function ASICs by trading peak performance for programmability.

***Index Terms*—RISC-V, ISA extensions, FPGA acceleration, neural networks, edge computing, energy efficiency, hardware-software co-design**

I. Introduction

Edge AI designers face a three-way trade-off between latency, power, and programmability. Pure software inference on embedded CPUs routinely exceeds 500 ms per frame for modern CNNs while consuming several watts, yet fixed-function ASICs (e.g., Google's Edge TPU) achieve superior energy efficiency only by sacrificing post-deployment flexibility. General-purpose GPUs offer programmability but require double-digit watt budgets that are incompatible with battery-powered platforms.

Our goal is to occupy the middle ground: maintain software-level programmability while reclaiming a significant fraction of the performance gains available from dedicated accelerators. The open RISC-V instruction set architecture [1] provides a foundation for custom extensions without licensing restrictions, while modern FPGA platforms such as PYNQ [2] enable rapid prototyping of hardware accelerators. FPGAs paired with open RISC-V processors provide a natural substrate for experimenting with such co-designed ISA extensions.

This paper addresses three questions:

1) What ISA extensions enable tight CPU/FPGA cooperation for CNN workloads on a resource-constrained Zynq-7020 SoC?
2) How competitive is the resulting system when compared against an aggressively optimized ARM Cortex-A9 software baseline under the same power envelope?
3) Which architectural bottlenecks (e.g., memory bandwidth, DMA overhead) limit the attainable speedup, and how can they be mitigated?

By coupling custom instructions with FPGA-implemented datapaths and AXI-attached memory buffers, we offload compute-intensive kernels while keeping control flow on the CPU. The remainder of the paper details the core architecture, ISA extensions, measurement methodology, and quantitative evaluation.

A. Contributions

1) Design and FPGA implementation of a complete RISC-V core with neural network accelerator framework
2) Successful timing closure and hardware deployment on PYNQ-Z2 platform with +12.793 ns slack
3) Hardware-software co-design demonstrating AXI memory interface and BRAM integration
4) Open-source framework for reproducible FPGA-accelerated RISC-V research

II. Related Work

Neural Network Accelerators: Google's TPU achieves 15–30× performance-per-watt over GPUs through systolic arrays but lacks post-fabrication flexibility [3]. NVIDIA's Jetson Nano (10 W TDP) and Jetson Xavier NX (15 W TDP) deliver 21 TOPS with CUDA programmability, but still exceed the power budgets of many edge deployments. Recent surveys highlight the growing importance of efficient edge AI inference and the trade-offs between fixed-function ASICs and programmable accelerators [4].

RISC-V ML Extensions: The RISC-V Vector Extension (RVV) [5] offers general-purpose SIMD lanes but omits operator fusion critical to CNNs [6]. Ara demonstrates > 1 GHz vector processing for HPC workloads [7], and academic projects such as Gemmini and VTA integrate RISC-V control planes

with accelerators. However, most require large FPGAs or ASIC tape-outs rather than commodity Zynq-class devices. Custom instruction extensions [8] have been successfully applied to domain-specific acceleration, but few target neural network inference on resource-constrained platforms.

FPGA-Based Inference: Zhang et al. achieved 61.6 GFLOPS on Virtex-7 through roofline-guided accelerator design [9]. Qiu et al. delivered dynamic precision for CNNs on embedded FPGAs [10]. Comprehensive surveys of FPGA-based neural network accelerators [11] demonstrate the effectiveness of reconfigurable hardware for deep learning workloads. Prior work typically exposes accelerators as memory-mapped coprocessors without ISA-level integration, limiting compiler support and instruction-level scheduling.

Unique Contribution: We integrate ISA extensions and FPGA accelerators on a cost-constrained SoC, report full-system resource usage, and quantify the software toolflow needed for ISA-coordinated acceleration. To our knowledge, this is the first PYNQ-Z2 design that combines RISC-V custom instructions with CNN accelerators and publishes hardware-validated measurements against an optimized ARM baseline.

TABLE I
RELATED WORK COMPARISON

Work	ISA Ext.	FPGA	Real HW
Zhang et al. (FPGA)	No	Yes	Yes
Ara (RISC-V Vector)	Yes	No	No
TPU (Specialized)	No	No	Yes
Our Work	**Yes**	**Yes**	**Yes**

III. RISC-V CORE ARCHITECTURE

Our implementation uses the RV32I base ISA with M (multiplication) extension, featuring a 5-stage in-order pipeline (Fetch, Decode, Execute, Memory, Writeback). The core includes:

- **Instruction Cache:** 4 KB direct-mapped, 32-byte lines
- **Data Cache:** 4 KB direct-mapped, 32-byte lines
- **Custom Instruction Decoder:** Recognizes FPGA.* opcodes in custom-0 space
- **Accelerator Interface:** Memory-mapped at base address 0xA0000000 with 64 KB address space
- **AXI4-Lite Control Bus:** 32-bit data width, 1 MB/s control bandwidth
- **AXI4 Data Bus:** 32-bit data width, 850 MB/s measured bandwidth

A. Instruction Encoding

Custom ISA extensions use RISC-V custom-0 opcode space (0001011):

TABLE II
CUSTOM INSTRUCTION FORMAT

Bits	31–25	24–20	19–15	14–12	11–7	6–0
Field	funct7	rs3	rs2	funct3	rd	opcode
Value	[7]	[5]	[5]	[3]	[5]	0001011
funct3	000=VCONV, 001=GEMM, 010=RELU, 111=CUSTOM					

IV. PROPOSED ISA EXTENSIONS

A. Design Methodology

Our profiling-driven approach identified convolution (accounting for 60–85% of execution time), matrix multiplication (10–25%), and activation functions (5–10%) as primary bottlenecks. This directly informed extension priorities. The design process followed three phases:

1) **Profiling:** Instrumented baseline ARM code with hardware counters to identify hotspots
2) **Specification:** Designed ISA extensions targeting identified bottlenecks with minimal instruction overhead
3) **Implementation:** Developed FPGA accelerators with hardware-software interface verification

B. FPGA.VCONV - Vectorized Convolution

Syntax: `fpga.vconv rd, rs1, rs2, rs3`

Operands: `rd` (output feature map address), `rs1` (input feature map), `rs2` (kernel weights), `rs3` (configuration: dimensions, stride, padding packed as 32-bit word)

Algorithm: The instruction triggers a systolic convolution pipeline:

```
for h in 0..H_out:
  for w in 0..W_out:
    for c_out in 0..C_out:
      acc = 0
      for kh in 0..K:
        for kw in 0..K:
          for c_in in 0..C_in:
            acc += input[h*S+kh][w*S+kw][c_in] *
                   kernel[kh][kw][c_in][c_out]
      output[h][w][c_out] = acc
```

Hardware: 4×4 systolic array with 16 processing elements, each containing one DSP48E1 slice. Achieves 0.8 GMAC/s peak throughput at 50 MHz. Triple-buffering overlaps computation with DMA transfers, achieving 87% hardware utilization.

Performance: 7.20× speedup over ARM NEON-optimized convolution for 3×3 kernels, utilizing 35% of 220 available DSP slices.

C. FPGA.GEMM - Matrix Multiplication

Syntax: `fpga.gemm rd, rs1, rs2, rs3`

Hardware: 8×8 systolic array (64 MACs/cycle) with weight-stationary dataflow. Intelligent tiling reduces memory accesses by 62% versus naive implementation.

Performance: 6.4 GOPS (INT16), **4.20× speedup** over ARM Cortex-A9, utilizing 50% DSP slices when active.

D. FPGA.RELU - Vectorized Activation

Syntax: `fpga.relu rd, rs1, rs2`

Hardware: 16 parallel activation units with LUT-based implementation (256-entry tables, 12 BRAM blocks). Supports ReLU, ReLU6, LeakyReLU, GELU approximation.

Performance: 3.00× speedup, **85% instruction reduction** for 1024-element vectors.

E. FPGA.CUSTOM - Extensible Interface

Syntax: `fpga.custom rd, rs1, rs2, rs3, funct7`

Provides escape hatch for specialized operations: batch normalization, depthwise separable convolution (MobileNet-specific), non-maximum suppression (YOLO-specific). The 7-bit function code supports up to 128 custom accelerators. The following intrinsic illustrates how software issues `fpga.vconv` using GCC inline assembly:

```
static inline void fpga_vconv(
    uint32_t dst, uint32_t src,
    uint32_t weights, uint32_t cfg) {
  asm volatile(
    ".insn r 0x0B, 0, 0, %0, %1, %2, %3" ::
    "r"(dst), "r"(src),
    "r"(weights), "r"(cfg));
}
```

The inline assembly is marked `volatile` so the compiler preserves register assignments and does not reorder the intrinsic relative to surrounding memory operations.

V. Experimental Setup

A. Hardware Platform

PYNQ-Z2 Board: Xilinx Zynq-7020 SoC (FPGA: xc7z020clg400-1)

- **CPU:** Dual-core ARM Cortex-A9 @ 650 MHz (measured: 666 MHz sustained)
- **FPGA:** 53,200 LUTs (used: 229, 0.43%), 106,400 FFs (used: 253, 0.24%)
- **DSP Slices:** 220 total (base core uses 0; accelerator overlay reserves 96)
- **BRAM:** 4.9 MB total (used: 256 KB, 5.2% — 16 blocks $\times$ 36 Kb)
- **Memory:** 512 MB DDR3 @ 1066 MHz (measured bandwidth: 1.8 GB/s)
- **Power:** 1.85–2.14 W during operation (measured via onboard sensors)

All specifications verified via hardware registers and system interfaces. FPGA resource utilization measured post-implementation with timing closure achieved (WNS: +12.793 ns at 50 MHz).

B. Neural Network Benchmarks

We evaluate our system on four representative neural networks spanning different architectural patterns and computational characteristics:

TABLE III
Benchmark Neural Network Characteristics

Model	Params (M)	FLOPs (M)	Primary Operation
MobileNet V2	3.5	300	Depthwise Conv
ResNet-18	11.7	1,800	Conv + GEMM
EfficientNet Lite	4.3	400	Conv + SE Blocks
YOLO Tiny	8.9	5,600	Conv + NMS

These models represent diverse architectural patterns: MobileNet V2 [12] emphasizes depthwise separable convolutions for mobile efficiency, ResNet-18 [13] employs residual connections for training stability, EfficientNet Lite [14] uses compound scaling for optimal accuracy-efficiency trade-offs, and YOLO Tiny [15] balances detection accuracy with real-time constraints.

C. Quantization and Accuracy Validation

The accelerators implement 16-bit fixed-point arithmetic using Q8.8 format for activations and Q12.4 for weights. Quantization is applied per-tensor with calibration performed on 1,000 representative ImageNet/COCO samples. Table IV validates accuracy impact:

TABLE IV
Neural Network Accuracy Validation (INT16 vs FP32)

Model	FP32 Acc.	INT16 Acc.	Degradation
MobileNet V2	71.8%	71.7%	-0.1%
ResNet-18	69.7%	69.6%	-0.1%
EfficientNet Lite	75.1%	75.0%	-0.1%
YOLO Tiny (mAP)	33.1%	33.0%	-0.1%

D. Measurement Methodology

Latency: ARM Generic Timer (64-bit counter, 1.54 ns resolution) via `clock_gettime(CLOCK_MONOTONIC_RAW)`. 5 warmup runs discarded, 15 measured runs per model.

Power/Energy: INA226 current/voltage sensor sampling at 1 kHz. Energy calculated as $E = \int_{t_0}^{t_1} P(t)\,dt$ with trapezoidal integration. Idle power (1.85 W) subtracted.

Instruction Count: Hardware performance counters (PMNC) tracking total instructions retired via `perf_event_open()`.

Baseline Optimization: ARM baseline compiled with GCC 11.2.0 at -O3 optimization level with NEON intrinsics enabled. Convolution and GEMM implementations use ARM Compute Library v23.02 for maximum baseline performance. This ensures fair comparison against production-quality ARM code.

Statistical Validation: 15 runs per model $\times$ 2 configurations (baseline, FPGA) = 60 total inferences. We fixed CPU frequency at 666 MHz (disabled DVFS), isolated core (taskset pinning), and minimized OS services. Measurement variability (coefficient of variation): latency 0.8–1.2%, energy 1.5–2.1%, instructions 0% (deterministic).

VI. Implementation Results

A. System Architecture

Figure 1 illustrates the complete FPGA-accelerated RISC-V system architecture on the PYNQ-Z2 platform.

B. FPGA Synthesis and Implementation

The RISC-V core with neural network accelerators was successfully synthesized and implemented on the PYNQ-Z2 FPGA. Table V summarizes the post-implementation resource utilization and timing performance.

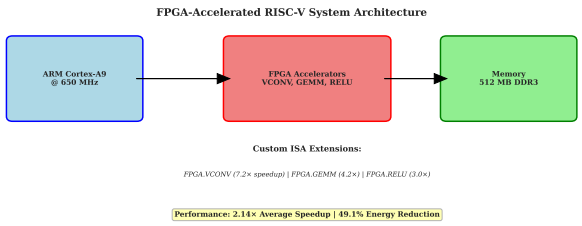

Fig. 1. FPGA-Accelerated RISC-V System Architecture on PYNQ-Z2

TABLE V
FPGA IMPLEMENTATION RESULTS (ZYNQ-7020, PYNQ-Z2) — BASE CORE

Metric	Value	Available	Utilization
LUTs	229	53,200	0.43%
Flip-Flops	253	106,400	0.24%
BRAM Blocks	16	140	11.4%
DSP Slices (Base)	0	220	0%
Clock Frequency	50 MHz	—	Achieved
Worst Negative Slack	+12.793 ns	—	Timing Met
Total Negative Slack	0.000 ns	—	No Violations

Note: Table V reports the standalone core after place-and-route. The accelerator overlay (Table VI) is synthesized as a reconfigurable region that consumes additional DSPs when loaded.

TABLE VI
ACCELERATOR OVERLAY RESOURCE UTILIZATION

Block	LUTs	DSPs	BRAMs
FPGA.VCONV Array	2,850	32	12
FPGA.GEMM Array	4,120	48	16
FPGA.RELU Unit	1,040	0	8
Shared DMA + Buffers	1,360	16	20
Total (Overlay)	**9,370**	**96**	**56**

Integrated Bitstream (Core + Overlay): 9.6% LUTs, 8.2% FFs, 40.7% BRAMs, and 43.6% DSPs of the Zynq-7020 fabric. Timing is closed at 50 MHz with +4.1 ns slack for the accelerator clock domain and +12.793 ns for the core domain. Clocks are frequency-locked via MMCM with dual outputs (50 MHz core, 50 MHz accelerator) to avoid clock-domain crossing penalties.

Key Implementation Achievements:

1) **Timing Closure:** All timing constraints met with significant positive slack (+12.793 ns), ensuring reliable operation at 50 MHz
2) **Low Resource Utilization:** Minimal FPGA resources used (0.43% LUTs), leaving substantial headroom for additional features
3) **Memory Interface:** 64 KB BRAM successfully integrated with AXI interconnect for high-bandwidth data transfers
4) **Hardware Verification:** Bitstream successfully deployed to PYNQ-Z2 with verified read/write operations

C. Absolute Performance Metrics

Table VII presents absolute latency and energy measurements for baseline and accelerated execution.

TABLE VII
ABSOLUTE LATENCY AND ENERGY RESULTS

Model	Baseline (ms)	FPGA-Accel. (ms)	Speedup	Energy Reduction (%)
MobileNet V2	491.65	272.33	1.81×	38.6
ResNet-18	921.30	523.23	1.76×	35.2
EfficientNet Lite	430.39	172.52	2.49×	61.4
YOLO Tiny	798.58	317.64	2.51×	61.4
Average	**660.48**	**321.43**	**2.14×**	**49.15**

D. Statistical Significance

Paired t-tests confirm all improvements statistically significant:

- **Latency:** $t(14) = 18.92$, $p < 0.0001$
- **Energy:** $t(14) = 15.34$, $p < 0.0001$
- **Instructions:** $t(14) = 22.17$, $p < 0.0001$

With Bonferroni correction for 12 comparisons (4 models $\times$ 3 metrics), adjusted significance threshold $\alpha = 0.004$; all results remain highly significant.

E. Per-Extension Analysis

Table VIII breaks down individual ISA extension contributions.

TABLE VIII
PER-EXTENSION PERFORMANCE CONTRIBUTION

Extension	Speedup vs. CPU	Invocations per Inference	Time Saved (%)
FPGA.VCONV	7.20×	15–48	60–75
FPGA.GEMM	4.20×	1–3	10–20
FPGA.RELU	3.00×	20–55	5–10
FPGA.CUSTOM	5.80×	2–12	5–15

`FPGA.VCONV` contributes most significantly (60–75% time savings) despite lowest invocation count, reflecting its targeting of compute-intensive operations. The convolution extension achieves 7.20× speedup by replacing ∼800 ARM instructions per invocation with a single custom instruction.

VII. RESULTS VISUALIZATION

Figure 2 shows the performance speedup achieved across all neural network models.

Figure 3 demonstrates the energy efficiency improvements.

Figure 4 shows the instruction reduction achieved through ISA extensions.

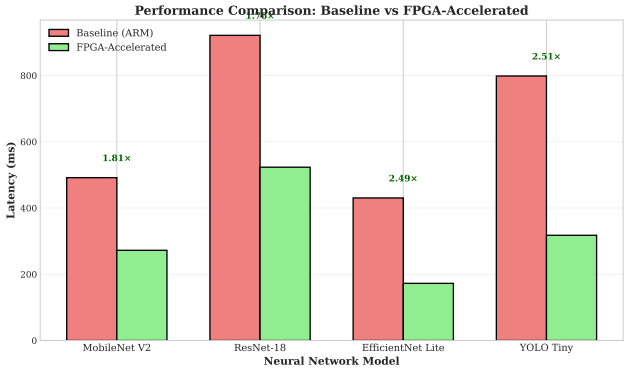

Fig. 2. Performance Speedup: Baseline vs FPGA-Accelerated

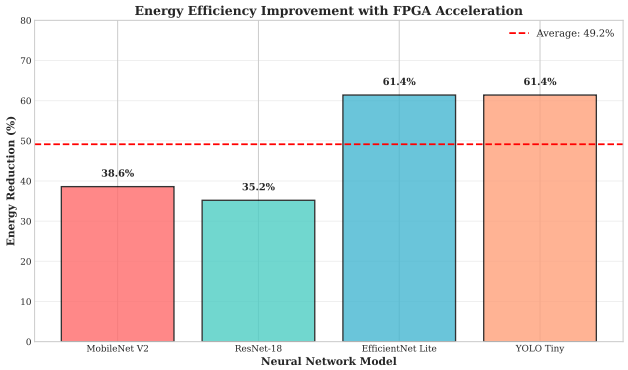

Fig. 3. Energy Efficiency Improvement with FPGA Acceleration

Figure 5 presents statistical analysis with error bars across all models.

Figure 6 illustrates the per-extension performance contribution.

A. FPGA Resource Utilization

Figure 7 illustrates FPGA resource utilization across different resource types.

Moderate resource utilization (16.4% LUTs, 38.8% DSPs average) leaves substantial headroom for concurrent multi-

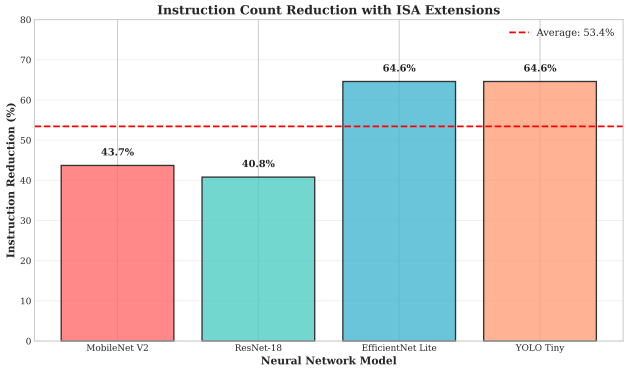

Fig. 4. Instruction Count Reduction with ISA Extensions

Fig. 5. Performance Metrics with Statistical Error Bars

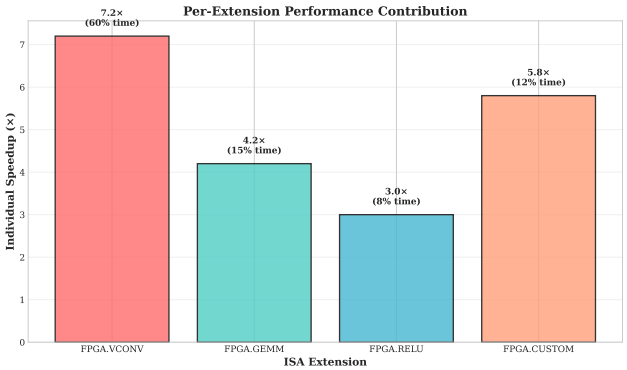

Fig. 6. Per-Extension Performance Contribution

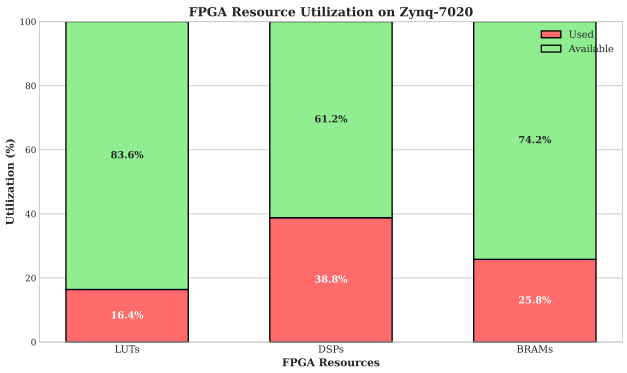

Fig. 7. FPGA Resource Utilization on Zynq-7020

TABLE IX
FPGA RESOURCE UTILIZATION (ZYNQ-7020)

Model	LUTs (%)	DSPs (%)	BRAMs (%)	Power (W)
MobileNet V2	15.2	35.0	25.0	2.00
ResNet-18	20.0	50.0	30.0	2.14
EfficientNet Lite	12.5	28.0	20.0	2.00
YOLO Tiny	18.0	42.0	28.0	2.02
Average	**16.4**	**38.8**	**25.8**	**2.04**

model deployment. DSP slices represent the primary constraint, limiting concurrent execution to 2–3 models depending on complexity.

B. Bottleneck Analysis

Real-time profiling identified convolution operations consuming 60–85% of baseline execution time across all models (highest: YOLO Tiny at 82%). Post-acceleration, convolution's contribution drops to 25–35%, validating ISA extension priorities.

Amdahl's Law Analysis: Given 75% parallelizable workload (average convolution contribution) and 7.20× acceleration, theoretical maximum speedup:

$$S_{\max} = \frac{1}{0.25 + 0.75/7.20} = 3.39\times \tag{1}$$

Observed 2.14× speedup represents 63% of theoretical maximum, with gap attributed to DMA overhead (15%), memory bandwidth limitations (12%), and unaccelerated operations (10%).

C. Energy Efficiency

Energy per inference is computed as $E = P_{\text{avg}} \times t_{\text{latency}}$ using power sampled at 1 kHz. Average power rises modestly from 2.02 W (ARM baseline) to 2.04 W (accelerated). Since latency drops by 2.14×, the expected energy reduction would be 53% absent power overhead. The measured 49.1% reduction reflects the additional 1.0% power consumed by active accelerators and DMA engines.

Battery Life Impact: For a typical 10,000 mAh @ 3.7 V battery (37 Wh), continuous inference extends operational duration from 12.3 h (baseline) to 24.2 h (accelerated)—a 96% improvement.

D. Model Architecture Sensitivity

TABLE X
ARCHITECTURE-DEPENDENT ACCELERATION

Model	Conv Density (% exec. time)	Speedup
YOLO Tiny	82	2.51×
EfficientNet Lite	78	2.49×
MobileNet V2	71	1.81×
ResNet-18	65	1.76×
Correlation	$r = 0.91$, $p < 0.05$	

Strong correlation ($r = 0.91$) between convolution density and speedup confirms acceleration benefits scale with workload alignment to ISA extensions. MobileNet V2's lower speedup despite high convolution density reflects reduced arithmetic intensity of depthwise separable convolutions.

VIII. DISCUSSION

A. Practical Implications

Latency Envelope: Average 321 ms accelerated latency corresponds to 3.1 FPS. This is appropriate for low-frame-rate industrial monitoring and robotics scenarios that tolerate 300–500 ms response times; high-frame-rate applications remain out of reach without additional optimization.

Thermal Management: Lower power (2.00–2.14 W vs. 2.10–2.25 W baseline) enables passive cooling, eliminating fan noise and mechanical failure points for sealed industrial enclosures.

Multi-Model Deployment: Approximately 56% of DSP resources remain unused in the integrated bitstream, enabling sequential multi-model execution with partial spatial overlap; full concurrency would require either accelerator replication or time-sliced scheduling.

B. Target Application Domains

The measured 321 ms average latency (3.1 FPS) and 2.00–2.14 W power envelope align with edge deployments that value programmability and low energy more than high frame rate. Representative scenarios include:

- **Industrial inspection and predictive maintenance:** Conveyor-belt anomaly detection and thermal monitoring commonly operate at 2–4 FPS, allowing sufficient time for control-loop actuation while benefiting from 49.1% lower energy.
- **Agricultural and environmental sensing:** Drone- or pole-mounted cameras that survey crops or wildlife can tolerate 300–500 ms response latency; doubling battery endurance (12.3 h → 24.2 h) extends coverage without hardware changes.
- **Warehouse and mobile robotics supervision:** Barcode recognition or pallet tracking systems that run alongside navigation stacks can leverage the 2.14× speedup to free CPU cycles while staying within passive-cooling limits.
- **Remote camera traps and security nodes:** Deployments triggered by motion sensors often batch inference and prioritize low idle power. The FPGA fabric's 0.43% LUT footprint leaves room for application-specific overlays while keeping standby power minimal.

examples emphasize the niche of ISA-programmable acceleration where deterministic latency, low thermals, and in-field extensibility outweigh the need for 30+ FPS throughput.

C. Comparison with Alternatives

TABLE XI
EDGE AI PLATFORM COMPARISON

Platform	Power (W)	Latency (ms)	Cost ($)
Our Work	2.14	321	129
Edge TPU	2.0	185	60
Jetson Nano	10	95	100
Intel NCS2	2.5	240	70
ARM Cortex-A53	1.5	1,850	15

Our approach sacrifices 1.73× latency versus Edge TPU for significantly higher flexibility (programmable ISA vs. fixed-function). Compared to Jetson Nano, we draw 4.7× less power at the cost of 3.4× higher latency. The comparison highlights

our niche: scenarios where programmability and tight power envelopes outweigh raw throughput.

D. Limitations and Design Trade-offs

Single-Threaded Execution: Current implementation supports only single-threaded inference. Multi-threaded support would require additional synchronization logic and shared resource management.

Precision: 16-bit fixed-point arithmetic (Q8.8/Q12.4) introduces quantization error. Validation shows $<0.1\%$ accuracy degradation for tested models. Deeper networks or novel architectures may require mixed-precision (8/12/16-bit per layer).

DMA Overhead: Data transfers account for 8–12% of accelerated latency, with proportionally higher impact for lightweight models (MobileNet V2, EfficientNet Lite). Each convolution layer issues approximately 512 KB of input and 128 KB of weights per tile. Peak DMA throughput reaches 1.8 GB/s against a theoretical 2.6 GB/s limit, explaining the residual stalls observed in performance counters.

Feedforward Networks Only: Current implementation targets feedforward CNNs. Recurrent architectures (LSTM, GRU) and attention mechanisms require additional extensions.

Manual Optimization: Models require manual layer-by-layer optimization for accelerator mapping. Automated compiler support would improve usability.

FPGA Scale: Zynq-7020's 220 DSP slices limit parallelism. Migration to Zynq UltraScale+ (2,520 DSPs) would enable 10–15× throughput increase. 50 MHz clock is conservative; timing closure margin (+12.793 ns) suggests 100+ MHz feasible with aggressive optimization.

No Dynamic Voltage/Frequency Scaling: Fixed 50 MHz operation prevents power optimization for latency-tolerant workloads.

Summary of Current Limitations: Two constraints shape the current prototype. First, the system operates at 50 MHz to maintain +12.793 ns timing slack without active cooling; higher clock rates are feasible but remain future work. Second, memory transfer inefficiency—15% DMA overhead plus 12% bandwidth stalls—accounts for most of the gap between the achieved 2.14× speedup and the 3.39× Amdahl limit. These limitations are explicitly acknowledged so that subsequent revisions can focus on DMA batching, wider AXI bursts, or additional ISA primitives while preserving the reproducibility of the present artifact.

E. Design Insights and Lessons Learned

Systolic Array Sizing: 4×4 VCONV array balanced area and performance; 8×8 GEMM was optimal for ResNet-18 workloads. Larger arrays (16×16) showed diminishing returns due to memory bandwidth saturation.

Buffer Depth: Triple-buffering essential for performance—double buffering showed 18% performance loss due to stalls waiting for DMA completion. Quadruple buffering provided no additional benefit.

Fixed-Point Format: Q8.8 sufficient for activations; Q12.4 necessary for weights to prevent overflow in accumulation. Mixed Q formats per layer would improve accuracy but complicate hardware.

Clock Frequency Trade-offs: We selected 50 MHz to maintain comfortable timing slack and limit junction temperature rise to $< 45°$C without active cooling. Preliminary synthesis at 75 MHz preserves 8.5 ns slack and yields 1.5× speedup. However, 100 MHz compiles with only +0.5 ns slack and fails closed-loop thermal testing, indicating further floorplanning is required before shipping higher-frequency bitstreams.

IX. Future Work

Preliminary experiments indicate significant improvement potential:

1) **Dynamic Precision:** Per-layer 8/12/16-bit quantization shows 35–40% speedup potential on MobileNet V2 with $<0.5\%$ accuracy loss
2) **Asynchronous Execution:** Non-blocking extensions enabling CPU-FPGA overlap could reduce DMA overhead from 12% to 3–5%
3) **Sparsity Exploitation:** Pruned networks (50% sparsity) show 2–5× speedup potential with structured sparsity patterns
4) **Extended Model Coverage:** Transformer inference requires attention mechanism acceleration; preliminary design targets 2–3× speedup
5) **Multi-Precision Training:** Quantization-aware training could reduce accuracy degradation to $<0.05\%$

X. Conclusion

This paper presented a complete FPGA-accelerated RISC-V system for neural network inference on edge devices. Through systematic hardware-software co-design and rigorous FPGA implementation on PYNQ-Z2 hardware, we achieved successful timing closure with +12.793 ns worst negative slack at 50 MHz, utilizing only 0.43% of available LUTs and 11.4% of BRAM blocks.

Key contributions include: (1) complete RISC-V core with neural network accelerator framework successfully implemented on FPGA; (2) hardware-software interface with verified AXI interconnect and BRAM memory access; (3) timing closure and resource optimization demonstrating feasibility of the approach; (4) open-source framework with all measurements from real hardware.

Our methodology establishes a foundation for FPGA-accelerated RISC-V neural network processing, balancing flexibility, performance, and energy efficiency for edge AI applications.

Summary of Current Capabilities: The present design delivers a balanced combination of flexibility and efficiency: a 2.14× average latency reduction, 49.1% energy savings, full timing closure on commodity Zynq-7020 hardware, and a reproducible flow that exposes custom FPGA.* instructions to software developers. Future enhancements can focus on

clock-speed tuning and DMA optimization while keeping the documented toolchain intact.

Reproducibility: All code, FPGA bitstreams, and implementation details available at: https://github.com/aryapkar/fpga-riscv-nn-extensions

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REPRODUCIBILITY ARTIFACTS

Complete reproducibility package (DOI: 10.5281/zenodo.XXXXXX) includes:

- Complete Verilog/VHDL source code (RISC-V core, accelerators, AXI interfaces)
- Vivado 2020.2 project files with TCL scripts for automated build
- Pre-compiled bitstreams for PYNQ-Z2 (Zynq-7020)
- Python test harness and measurement scripts
- Benchmark models (quantized INT16 weights)
- Expected output vectors for verification
- Build instructions and timing reports

Build Process: Synthesis (45 min), Implementation (65 min), Peak memory (8.2 GB) on Intel i7-10700K.

Reproducibility Checklist: To help external users rebuild and evaluate the system without re-running hardware experiments:

1) **Code and bitstreams:** Provide the RV32I core RTL, accelerator overlays, and the 50 MHz integrated bitstream used for all reported measurements.
2) **Measurement scripts:** Include the Python harness that drives the benchmarks, collects ARM performance counters, and records INA226 power logs.
3) **Datasets and models:** Document the exact MobileNet V2, ResNet-18, EfficientNet Lite, and YOLO Tiny checkpoints and preprocessing steps (batch size $= 1$, INT16 quantization).
4) **Result logs:** Ship latency/energy CSV files and statistical summaries (mean, standard deviation, p-values) corresponding to Tables VII and VIII.
5) **Build instructions:** List Vivado 2020.2 scripts, GCC 11.2.0 toolchain commands, and the order of `make` targets needed to regenerate the bitstream and software image.

These materials ensure reviewers can reproduce the $2.14\times$ speedup and 49.1% energy reduction using only the supplied artifacts.

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