

# Gate Dielectric Engineering with an Ultrathin Silicon-oxide Interfacial Dipole Layer for Low-Leakage Oxide-Semiconductor Memories

Fabia F. Athena,<sup>\*,†,||</sup> Jonathan Hartanto,<sup>\*,†,‡,||</sup> Matthias Passlack,<sup>¶</sup>

Jack C. Evans,<sup>†</sup> Jimmy Qin,<sup>†</sup> Didem Dede,<sup>‡</sup> Koustav Jana,<sup>†</sup> Shuhan Liu,<sup>†</sup>

Tara Peña,<sup>†</sup> Eric Pop,<sup>†</sup> Greg Pitner,<sup>¶</sup> Iuliana P. Radu,<sup>§</sup> Paul C. McIntyre,<sup>‡</sup> and

H.-S. Philip Wong<sup>\*,†</sup>

<sup>†</sup>*Department of Electrical Engineering, Stanford University, CA, USA*

<sup>‡</sup>*Department of Materials Science and Engineering, Stanford University, CA, USA*

<sup>¶</sup>*Corporate Research, Taiwan Semiconductor Manufacturing Company, Ltd., San Jose, CA, USA*

<sup>§</sup>*Corporate Research, Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan*

<sup>||</sup>*These authors contributed equally*

E-mail: fathena@stanford.edu; jh99@stanford.edu; hspwong@stanford.edu

## Abstract

We demonstrate a gate dielectric engineering approach leveraging an ultrathin, atomic layer deposited (ALD) silicon oxide interfacial layer (SiL) between the amorphous oxide semiconductor (AOS) channel and the high-k gate dielectric. SiL positively shifts the threshold voltage ( $V_T$ ) of AOS transistors, providing at least four distinct  $V_T$  levels with a maximum increase of 500 mV. It achieves stable  $V_T$  control without

significantly degrading critical device parameters such as mobility, on-state current, all while keeping the process temperature below 225 °C and requiring no additional heat treatment to activate the dipole. Positive-bias temperature instability tests at 85 °C indicate a significant reduction in negative  $V_T$  shifts for SiL-integrated devices, highlighting enhanced reliability. Incorporating this SiL gate stack into two-transistor gain-cell (GC) memory maintains a more stable storage node voltage ( $V_{SN}$ ) (reduces  $V_{SN}$  drop by 67%), by limiting unwanted charge losses. SiL-engineered GCs also reach retention times up to 10,000 s at room temperature and reduce standby leakage current by three orders of magnitude relative to baseline device, substantially lowering refresh energy consumption.

## Keywords

oxide semiconductor, gate-dielectric, multi- $V_T$ , dipole, interface,  $\text{SiO}_x$ , gain-cell

## Introduction

The persistent performance gap between processor speeds and memory bandwidth, commonly referred to as the "memory wall",<sup>1,2</sup> underscores the need for scalable, high-density, high-performance three dimensional (3D) chips enabled by back-end-of-line (BEOL) memory and logic. Amorphous oxide-semiconductor field-effect transistors (AOSFETs) are attractive for such BEOL integration due to compatibility with BEOL processes, low-temperature deposition, high-density integration potential, and excellent thickness uniformity achievable via atomic layer deposition (ALD) techniques.<sup>2–10</sup> Across envisioned uses—including 3D or 4F<sup>2</sup> (F is minimum feature size) dynamic random access memory (DRAM), ferroelectric field effect transistor (FeFET) based memory devices, power-delivery switches, and exploratory back-end-of-line (BEOL) logic—precise threshold-voltage ( $V_T$ ) control is indispensable.<sup>11–16</sup> For gain-cell (GC) memories<sup>6,17–19</sup> in particular,  $V_T$  directly sets retention time and write

margins. An excessively negative  $V_T$  increases subthreshold leakage and decreases retention time, whereas an overly positive  $V_T$  within a fixed operating voltage hampers charge transfer during write operations, making writes unreliable. Elevated temperatures exacerbate the  $V_T$  shift because additional thermal energy increases the concentration of oxygen vacancies and free carriers in the OS, driving  $V_T$  further negative.<sup>1,20–23</sup> Achieving control over  $V_T$  is therefore essential. Conventional  $V_T$ -tuning techniques such as doping, annealing, or passivation often introduce undesirable side effects, such as reduced field-effect mobility ( $\mu_{FE}$ ), degraded subthreshold slope (SS), and reliability issues linked to hydrogen release and bias instability.<sup>2,20,24–28</sup> In silicon MOSFETs, interface-dipole engineering shifts  $V_T$  positively or negatively via “p-type” or “n-type” dipoles by inserting ultrathin layers such as  $AlO_x$  or  $LaO_x$  into the gate stack, which sets an interfacial potential step that moves the channel band edges relative to the gate.<sup>29–34</sup> This offers a promising alternative approach for  $V_T$  control in two dimensional (2D) FETs.<sup>35,36</sup> In previous works,<sup>32</sup> we showed inserting  $AlO_x$  into the gate dielectric effectively shifts the  $V_T$  in AOS transistors.

In this work, we set out to investigate what other oxides could be used to tune  $V_T$  in the positive direction for AOS devices, to shed light on the use of a possible broader set of materials. This is also necessary to achieve volume-less  $V_T$  tuning for AOS gate-all-around (GAA) FETs. We study interface dipole engineering as a volume-less  $V_T$  tuning technique for amorphous indium-tungsten oxide (IWO) AOSFETs by integrating an ultrathin silicon oxide ( $SiO_x$ ) interfacial layer. Ultra-thin  $SiO_x$  layers are deposited via plasma-enhanced atomic-layer deposition (PEALD) at 200 °C without any additional annealing treatment. The SiL-engineered AOSFETs achieves positive shifts in  $V_T$  up to approximately 500 mV without significantly compromising device performance metrics, such as field effect mobility ( $\mu_{FE}$ ) or subthreshold slope (SS). Additionally, we evaluate the impact of the SiL on positive bias temperature instability (PBTI) at elevated temperature and demonstrate its effectiveness in mitigating negative  $V_T$  shifts under extended positive bias stress conditions. As an example of the application of this  $V_T$ -tuning technique, we integrated the SiL into a

two-transistor (2T) GC memory. Setting  $V_T$  higher significantly reduces the  $V_{SN}$  drop and substantially lowers leakage current, thereby improving retention and reducing refresh-energy requirements.

## Results and Discussion

Figure 1(a) shows the fabrication process flow of AOSFETs. For SiL-integrated devices, ultrathin  $\text{SiO}_x$  interfacial layers with thicknesses of 0.2 nm (SiL1), 0.6 nm (SiL2), and 0.9 nm (SiL3), 1.1 nm (SiL4) are deposited *in situ* with  $\text{HfO}_2$ . Details of the fabrication process are provided in the Supporting Information. Figure 1(b) schematically illustrates AOSFET structure incorporating the  $\text{SiO}_x$  based interfacial dipole layer which lies between the amorphous IWO channel and the high- $k$   $\text{HfO}_2$  gate dielectric. Figure 1(c) illustrates a 2T GC structure comprising a write transistor (WTR) and a read transistor (RTR). The source of the WTR is connected to the gate of the RTR forming a storage node (SN). Figure 1(d) provides the corresponding circuit diagram of 2T GC. Figure 1(e) shows a top-view atomic force microscope (AFM) image of the IWO channel in the OSFET, revealing a relatively smooth surface ( $R_q < 450 \pm 20$  pm). Details of the AFM procedure are described in the Supporting Information. A top view scanning electron microscope (SEM) in Figure 1(f) shows the layout of RTR, WTR, SN and read word line (RWL), read bit line (RBL), write word line (WWL), and write bit line (WBL). Details of the SEM measurement are provided in the Supporting Information. Figure 1(g) presents a cross-sectional transmission electron microscope (TEM) image of the fabricated device structure, which shows well-defined layers of IWO channel,  $\text{HfO}_2/\text{SiO}_x$  gate stack and Pt back-gate electrodes. Energy-dispersive spectroscopy (EDS) elemental mapping further confirms the uniform deposition and precise composition of different layers across the device stack as shown in Figure 1(h).

Figure 2(a) shows the transfer characteristics of baseline device (BL) and SiL-engineered AOSFETs. A clear positive shift in  $V_T$  is observed in the SiL-integrated devices relative to

the BL devices, reaching a maximum increase of  $\sim 500$  mV.  $V_T$  was extracted using constant current method at  $100 \text{ nA} \cdot \text{Width/Length}$  (near subthreshold), to include the effects of conduction via shallow band-tail states, which is characteristic of amorphous OS.<sup>37</sup> The observed positive shift in  $V_T$  is likely attributed to the formation of a positive interface dipole which drives  $V_T$  shift in the positive direction. We tentatively attribute the observed  $V_T$  shift in SiL devices to an interface dipole. This interpretation is supported by the saturation of  $V_T$  shift beyond a certain dipole layer thickness and our previous extensive investigation using an alternative  $\text{AlO}_x$  interfacial dipole layer,<sup>32</sup> which showed that  $\text{AlO}_x$  induced  $V_T$  shift is dipole-driven rather than caused by fixed charge, nevertheless further analysis is required. This dipole introduces a built-in electrostatic potential that raises the OS-channel energy bands relative to the gate, increasing the gate bias required to turn the device on. Importantly, as shown in Figures 2(b–d), integrating the SiL has minimal impact on critical device parameters, such as  $\mu_{\text{FE}}$  and SS, confirming precise  $V_T$  modulation without performance degradation.

Figure 2(e) presents ultraviolet photoelectron spectroscopy (UPS) spectra for  $\text{HfO}_2/\text{IWO}$  and  $\text{SiO}_x/\text{IWO}$  stacks, acquired under a negative sample bias ( $-10 \text{ V}$ ) to expose the secondary electron cutoff. Details of the UPS measurement is provided in the Supporting Information. The inset shows a zoomed view of the cutoff region used to extract the work function by linear extrapolation of the intensity–kinetic energy edge. The  $\text{SiO}_x/\text{IWO}$  stack exhibits a higher work function ( $4.08 \text{ eV}$ ) than  $\text{HfO}_2/\text{IWO}$  ( $3.87 \text{ eV}$ ), aligning with the experimentally observed higher  $V_T$  for the SiL-engineered devices. Figure 2(f) shows the simulated energy-band diagram obtained from a one-dimensional Poisson solver for the SiL stacks. Dirichlet boundary conditions are applied at the gate electrode and in the quasi-neutral semiconductor, with a Neumann (zero-flux) condition at the far boundary conditions are used only where a metal/semiconductor contact is explicitly included. The interface dipole is implemented as an interfacial potential step equivalently, two interfacial charge sheets of opposite polarity similar to Figure 2(f), producing an upward band shift on the OS side of

about 0.4 V compared to the baseline case and corroborating the proposed dipole-induced  $V_T$  modulation in the SiL devices. Details of the calculations are provided in the Supporting Information. Figure 2(f) compares the  $\Delta V_T = V_T - V_{BL}$ , for devices employing  $\text{SiO}_x$  and an alternate interface dipole material ( $\text{AlO}_x$ ). Except at a dipole thickness of 0.6 nm, where  $\text{AlO}_x$  shows a slightly larger  $\Delta V_T$ , the  $\text{SiO}_x$  cases exhibit higher  $\Delta V_T$  as a function of thickness, most noticeably at the saturation point (by  $\sim 50$  mV). This modest difference is possibly due to lower dielectric constant of  $\text{SiO}_x$ . The dipole strength is expected to be governed primarily by charge-neutrality-level (CNL) alignment at the OS/dielectric interface, because OS materials typically possess higher defect densities (and thus more gap states) than dielectrics, the interfacial CNL is more strongly influenced by the OS than by the dielectric. This interpretation is consistent with our prior experiment,<sup>32</sup> in which varying the OS while using an  $\text{AlO}_x$  dipole resulted in substantially larger  $\Delta V_T$  shifts compared to the change of dipole layer material in this work. Nevertheless, further theoretical and experimental studies are necessary to clarify the microscopic origin of the interface dipole and its interplay with different dielectrics. However, precise  $V_T$  tuning is achievable through the use of different dipole materials, offering a clear advantages for advanced 3D transistor structures, including gate all around structures.

To evaluate reliability, positive bias temperature instability (PBTI) measurements were conducted at elevated temperatures (85 °C) under the DC/worst case condition with three different overdrive biases ( $V_{ov} = 0.05$  V, 1.0 V, 2.0 V), as shown in Figure 3 (a,b). BL devices exhibit a significant negative  $V_T$  shift when  $V_{ov} = 2.0$  V is applied for 10,000 s, an effect attributed to hydrogen release from the gate dielectric. The released hydrogen (H) can either incorporate interstitially or bind at the oxygen vacancies, where it acts as a shallow donor.<sup>1,38,39</sup> Each incorporated H contributes an electron to the conduction band, effectively increasing the net donor density in the channel.<sup>1,40,41</sup> Conversely, SiL-integrated devices exhibited a small to moderate positive  $V_T$  shift after stress, indicative of electron trapping rather than H release. Arrhenius-based fits point to a moderately active electron

trapping pathway competing with a weaker H release pathway, producing only a modest net shift and improved reliability at the highest  $V_{ov}$  and long stress times in SiL devices.

Devices incorporating an alternative  $AlO_x$  dipole layer (AIL) demonstrate a significantly reduced negative  $V_T$  shift at the strongest bias stress voltage (Figure 3(c)) that also indicates electron trapping however, to a lesser extent than the  $SiO_x$  case. As mentioned before, the measured data were fitted to an Arrhenius-based reliability model<sup>1</sup> to gain deeper insight into the underlying degradation mechanisms, as indicated by the dashed lines in Figure 3(a)-(c). Arrhenius-based fits point to a weaker electron-trapping pathway competing with a field-assisted release process, this interplay yields only a small net shift and a much reduced negative shift, at the highest  $V_{ov}$ . Detailed descriptions of the fitting models and the extracted parameters are provided in the Supporting Information (S6). At room temperature, BL device typically show positive  $V_T$  shift. Stress-induced  $\Delta V_T$  arises from competition between electron trapping and hydrogen (H)-release-driven electron donation. Arrhenius fitting<sup>42,43</sup> shows that BL devices are dominated by H-release, leading to large negative shifts, while charge trapping is effectively suppressed. For SiL, both trapping and release mechanisms are active and their competition results in a moderate positive  $\Delta V_T$  at high stress times. AIL shows minimal activity from the positive and negative shift mechanisms, at high  $V_{ov}$  and long stress times, this device shows a very low magnitude  $\Delta V_T$  with the sign dependent on  $V_{ov}$ . Both SiL and AIL layers exhibit smaller  $V_T$  shifts and thus improved PBTI behavior compared to the baseline, however, further investigation is required and will be reported in a sequel to this work.

Figure 4 illustrates the measured transient characteristics of SiL-engineered GCs and baseline GCs. Figure 4(a)(i) shows the applied waveforms for the wordlines and bitlines. To enable multibit data storage, different data voltages  $V_{data}$  ranging from 1.4 V to 1.8 V are applied at the WBL. The corresponding read bit line current ( $I_{RBL}$ ) is shown in Figure 4(a)(ii), while the extracted  $V_{SN}$  is shown in Figure 4(a)(iii). The  $V_{SN}$  decay occurs in two distinct stages. First, a rapid voltage drop coincident with the falling edge of the

WWL pulse (red region), the voltage difference between the applied  $V_{\text{data}}$  and resulting  $V_{\text{SN}}$  after the initial fast drop process is defined as  $V_{\text{SNfast}}$ .

The rapid  $V_{\text{SNfast}}$  drop is primarily attributed to two mechanisms (1) capacitive coupling between the WTR to the SN,<sup>6</sup> and (2) mobile charge partitioning from write transistor (WTR) to the WBL and SN. Prior to the WWL falling edge, the WTR channel is in strong accumulation, all trap states in the bandgap are filled and excess carriers accumulate in the conduction band.<sup>44</sup> When the WWL voltage drops, the accumulated mobile charge in the WTR channel starts to deplete and flows toward the WBL and SN. Thus, more positive  $V_{\text{T}}$  of the WTR implies reduced charge partitioning. The  $V_{\text{SNfast}}$  is followed by a second stage of gradual decay ( $V_{\text{SNslow}}$ ) (green region). Quantitatively, a reduction of  $\sim 67\%$  in the total  $V_{\text{SN}}$  drop is observed for SiL GCs relative to their BL counterparts at WBL data level of 1.8 V. This improvement primarily arises from reduced subthreshold leakage currents and suppressed mobile charge injection enabled by the positive shift in  $V_{\text{T}}$  through SiL dipole engineering. As a result, the SiL leveraged positive  $V_{\text{T}}$  GCs exhibit a significantly lower overall  $V_{\text{SN}}$  drop compared to BL GCs.

Figure 5(a) details the bias conditions applied during retention measurements. During the standby condition the WWL is held at  $-0.5$  V. Figure 5(b) demonstrates that SiL GCs achieve significantly improved retention of up to 10,000 seconds, an improvement over BL GCs which show retention of  $< 2,500$  s. Additionally, retention characteristics for various SiL GCs with different threshold voltages were measured up to 2,000 seconds, as shown in Figure 5(c). Leakage currents (storage node leakage) are extracted from retention measurements by measuring the time elapsed for  $V_{\text{SN}}$  to drop by 0.1 V (Figure 5(d)) from the initial state. An exponential reduction in leakage current with increasing  $V_{\text{T}}$  is observed in SiL GCs, yielding lower leakage with roughly three orders of magnitude lower than in BL GCs. This directly translates to a significant decrease in refresh-energy demand and an improvement in overall memory efficiency.

# Conclusion

We demonstrated a volume-less  $V_T$  tuning method for amorphous AOSFETs by inserting an ultrathin  $\text{SiO}_x$  interfacial dipole layer (SiL) in the gate dielectric. The SiL provides a controllable positive  $V_T$  shift without degrading  $\mu_{\text{FE}}$  or SS, and it suppresses the negative  $V_T$  drift under worst-case DC PBTi at 85°C. In a 2T GC memory, the SiL stack reduces the  $V_{\text{SN}}$  drop by  $\sim 67\%$  versus BL GCs by limiting mobile-charge sharing and extends retention beyond  $10^4$  s, thereby reducing refresh energy.

Relative to our previous work on an  $\text{AlO}_x$  dipole-engineered dielectric,<sup>32</sup> we investigated  $\text{SiO}_x$  to probe how interfacial chemistry (lower  $k$  and different electronegativity) governs dipole-induced  $V_T$  control and to explore additional candidates for  $V_T$  tuning in oxide semiconductors. Experimentally,  $\text{SiO}_x$  yields a slightly higher  $V_T$  increase—by  $\sim 120$  mV compared with  $\text{AlO}_x$ —suggesting likely a different effective dipole strength. Whether this magnitude matches simple dipole-strength expectations remains an open question, further investigation is required. Possible next steps include developing a fundamental understanding of the  $V_T$  change with  $\text{SiO}_x$  via modeling and controlled thickness-series experiments, and coupling first-principles calculations with device electrostatics to predict the sign and magnitude of shifts. Establishing these fundamentals for  $\text{SiO}_x$  will solidify interfacial-dipole engineering as a rigorous, volume-less  $V_T$  tuning knob. Because it adjusts  $V_T$  without altering channel volume, stoichiometry, or doping, this approach is CMOS-compatible and scalable—opening a practical path to back-end compatible dual gate or GAA oxide-semiconductor transistors for high-speed, energy-efficient embedded 3D memory, consistent with the N3XT 3D vision.<sup>45,46</sup>

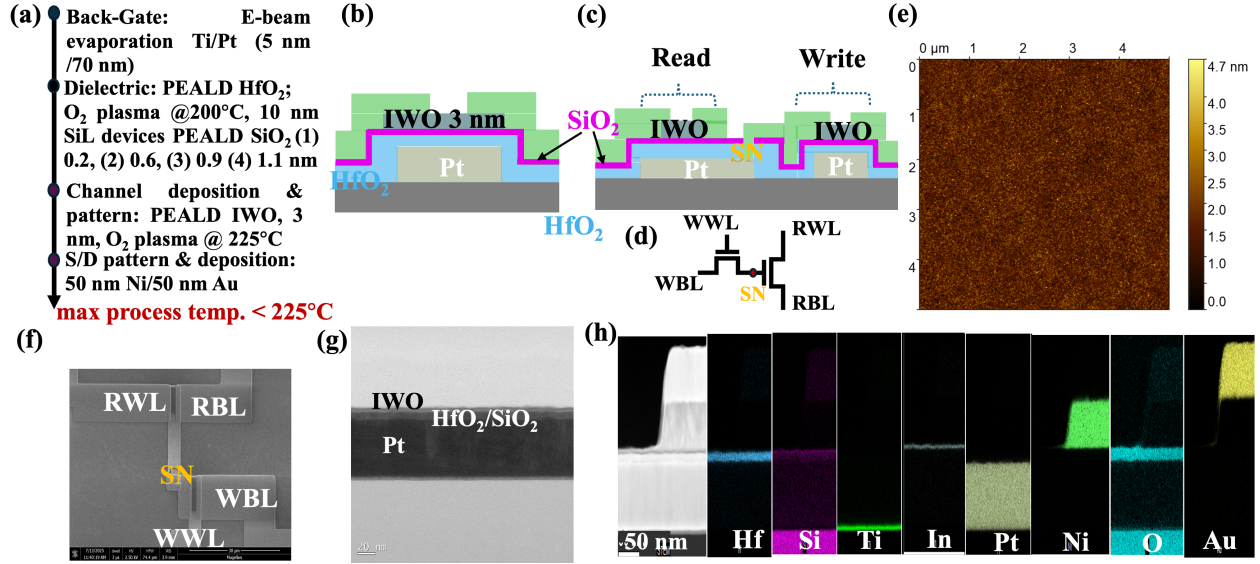


Figure 1: (a) Fabrication process flow of AOSFETs. Schematic illustration of (b) FET structure incorporating a SiO<sub>x</sub> dipole layer, (c) 2T GC, where the source of the WTR is connected to the gate of the RTR. (d) Circuit diagram of the corresponding n-n 2T GC highlighting the SN. (e) Top-view AFM image of IWO channel showing smooth surface of the film, revealing a relatively smooth surface ( $R_q < 450 \pm 20$  pm). (f) Top view SEM image of the fabricated GC showing RWL, RBL, WWL and WBL. Source of the write transistor is connected to the gate of the read transistor through SN. (g) Cross-sectional TEM image of the FET structure. (h) EDS elemental mapping illustrating uniform distribution of Hf, Si, Ti, In, Pt, Ni, O, and Au across the device cross-section.

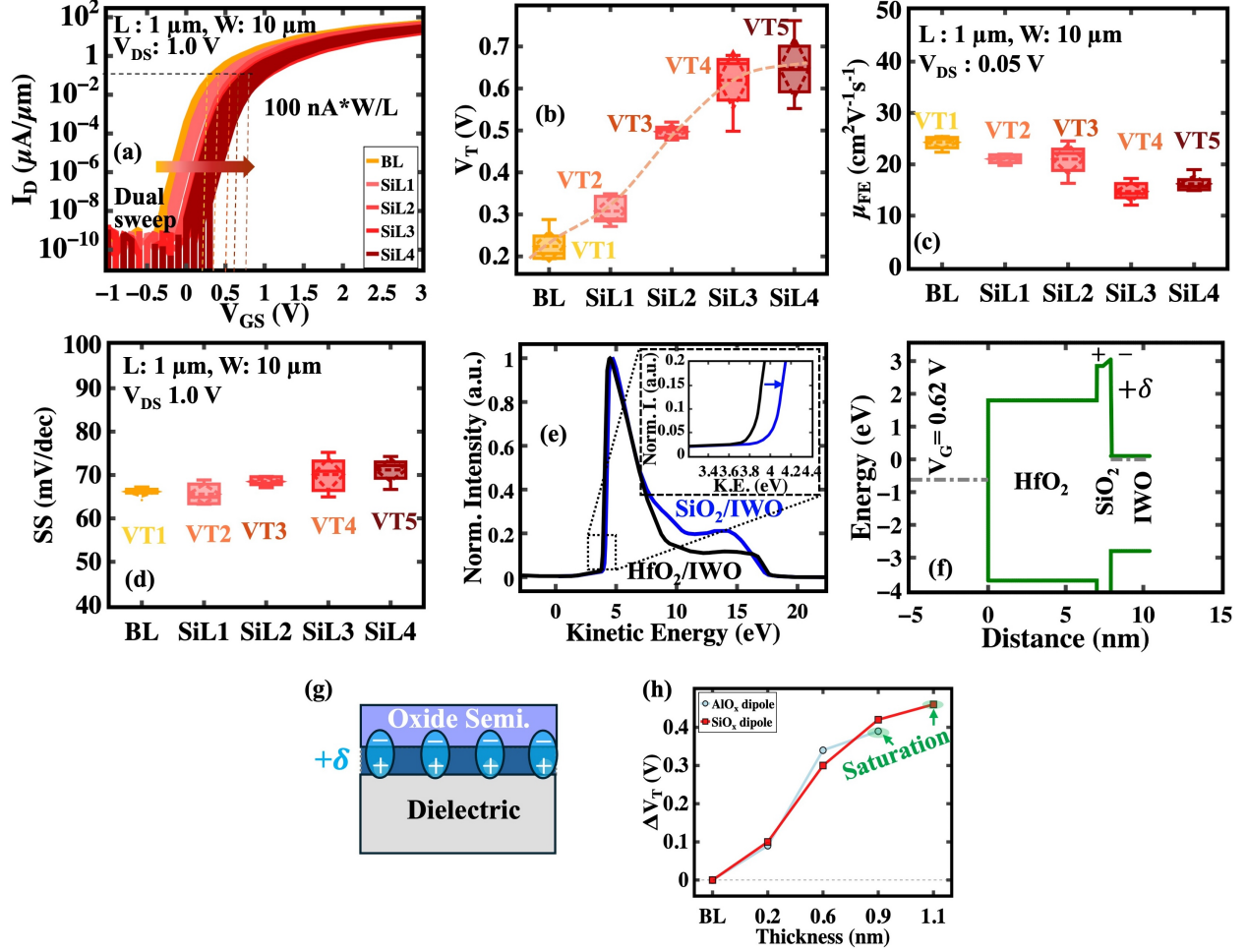


Figure 2: (a) Transfer characteristics ( $I_D$ - $V_{GS}$ ) of the BL and SiL device, measured at  $V_{DS}$  1 V. Here  $L = 1 \mu m$  and  $W = 10 \mu m$ . SiL devices clearly exhibit a positive  $V_T$  shift. (b)  $V_T$  distributions for different devices, showing that SiL devices achieve a maximum  $V_T$  increase of  $\sim 500$  mV compared to the BL. Here,  $V_T$  was extracted using constant current method at  $100 nA \cdot Width/Length$ . (c)  $\mu_{FE}$  of different devices indicate that  $\mu_{FE}$  remains largely unaffected by the SiL integration. (d) SS values of BL and SiL devices are within acceptable variation range. (e) UPS spectra acquired under applied bias (-10 V) for HfO<sub>2</sub>/IWO and SiO<sub>2</sub>/IWO samples. Inset shows zoomed view of the secondary electron cut-off region. The SiO<sub>2</sub>/IWO exhibits a higher work-function (4.08 eV) than HfO<sub>2</sub>/IWO (3.87 eV). (f) Simulated energy band-diagram of SiL OSFET obtained using one dimensional (1D) Poisson solver. (g) A positive dipole forms at the SiO<sub>2</sub>/IWO interface. (h) Comparison of  $\Delta V_T = V_T - V_{BL}$ , for devices employing SiO<sub>x</sub> and an alternate interfacial dipole material (AlO<sub>x</sub>). Except at a dipole thickness of 0.6 nm, where AlO<sub>x</sub> shows a slightly larger  $\Delta V_T$ , the SiO<sub>x</sub> cases exhibit higher  $\Delta V_T$  as a function of thickness, most noticeably at the saturation point (by  $\sim 50$  mV).

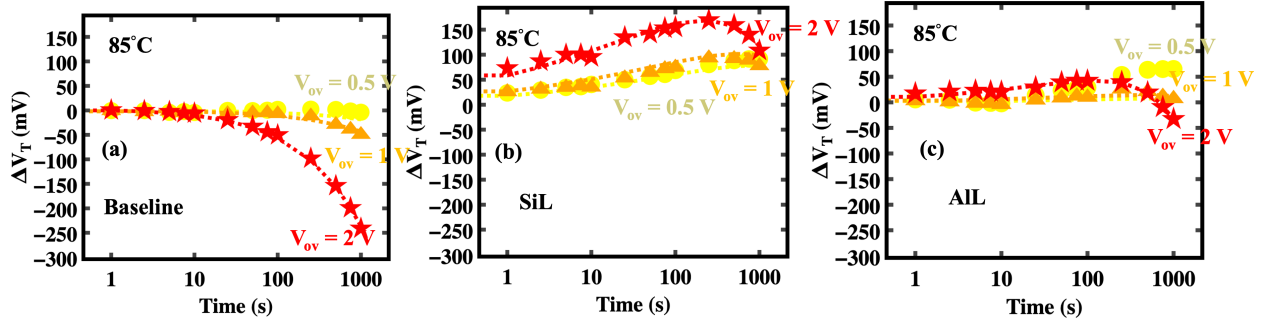


Figure 3: Positive-bias temperature instability of AOSFETs with and without dipole layers, stress applied up to 1000 s at 85 °C under over-drive biases of 0.5 V, 1.0 V, and 2 V. The dashed lines represent the model fits. (a) BL devices show a negative  $V_T$  shift of  $\sim -300$  mV at 2 MV/cm, attributed to hydrogen release from the gate dielectric that creates donor-like defects. (b) Dipole-engineered SiL devices exhibit a positive  $V_T$  shift of  $\sim 150$  mV, indicating that the  $\text{SiO}_x$  interfacial layer shifts the dominant degradation mechanism to electron trapping. (c) Devices with an  $\text{AlO}_x$  interfacial dipole layer show a smaller negative  $V_T$  shift of around -43 mV at  $V_{ov}$  of 2 V at 1000 s. Both  $\text{SiO}_x$  and  $\text{AlO}_x$  interfacial dipole layers eliminate the large negative  $V_T$  shift observed in BL devices enabling improved reliability.

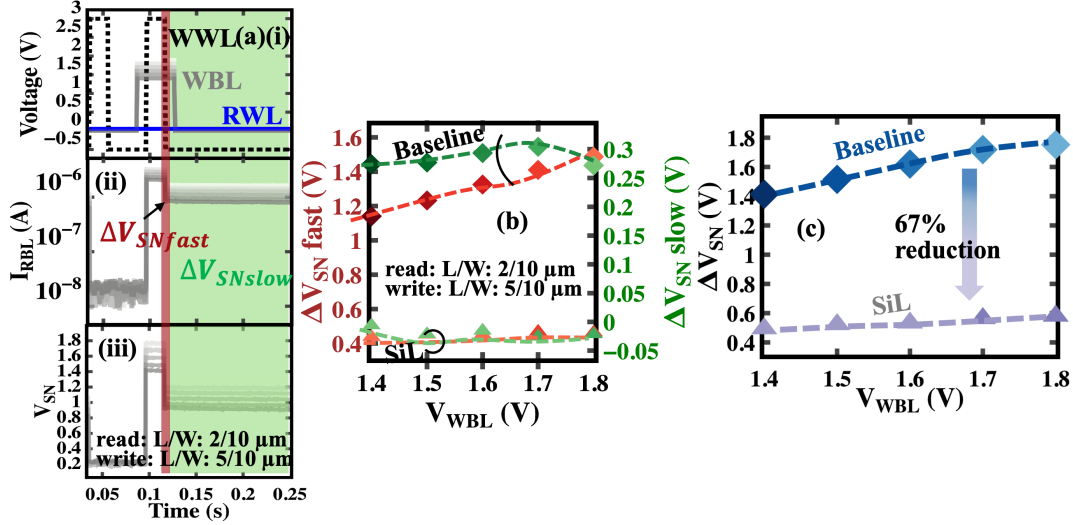


Figure 4: Timing diagram for the BL and SiL GC memory. (a) Measured waveforms as a function of time: (i) WWL, WBL, and RWL voltages, (ii)  $I_{RBL}$ , and (iii) storage-node voltage  $V_{SN}$ .  $V_{SN}$  decays in two stages: an immediate “fast” drop coincident with the falling edge of the WWL (red region), followed by a “slow” drop driven by post-write leakage (green region). (b) Distributions of the fast and slow components of  $V_{SN}$  loss for BL and SiL GCs. SiL GCs show lower  $V_{SN}$  drop compared to BL GCs. (c) Distribution of the total  $V_{SN}$  drop. The fast component is governed by the write-transistor  $V_T$ ; the higher  $V_T$  achieved with the  $\text{SiO}_x$  interfacial layer suppresses mobile charge sharing from the WTR to the SN and WBL, reducing both fast and overall  $V_{SN}$  drops relative to the BL.

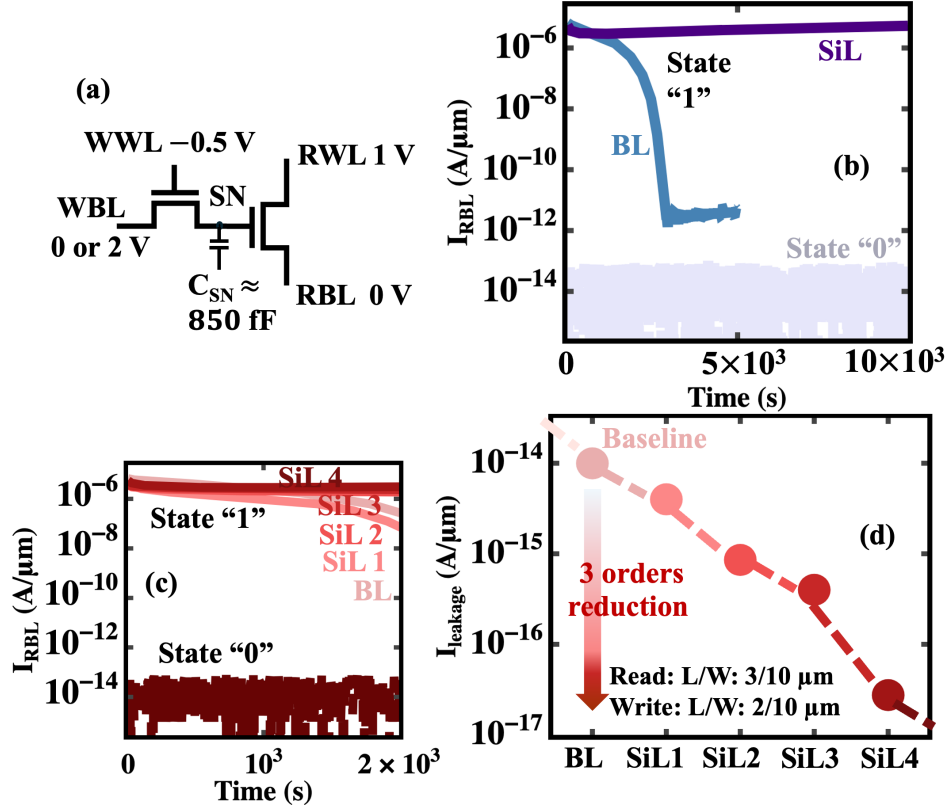


Figure 5: Retention performance of baseline and SiL GCs. (a) Bias condition during standby; WWL is held at  $-0.5$  V. Here, RTR  $L = 3$   $\mu$ m,  $W = 10$   $\mu$ m, WTR  $L = 2$   $\mu$ m,  $W = 10$   $\mu$ m. (b) The  $\text{SiO}_x$ -dipole GC SiL4 shows improved retention (up to 10 000 s) compared to BL GC. (c) State-1 retention for the BL and various SiL GCs, measured for 2000 s; State-1 is reported because it is the critical state and typically degrades fastest. (d) Leakage current extracted from  $V_{SN}$  degradation (defined as a 0.1 V drop from the initial value) for BL and SiL GCs. Leakage decreases exponentially with increasing  $V_T$  in the SiL GCs, achieving a three-order-of-magnitude reduction in the SiL4 GCs.

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