

Development of 3D Pixel Sensors via an 8-inch CMOS-Compatible Process

Huimin Ji, Zhihua Li, Wenzheng Cheng, Zheng Li, Kai Huang, Jing Wen, Song Liu, Manwen Liu, and Jun Luo

Abstract—In the construction of High-Luminosity Large Hadron Collider (HL-LHC) and Future Circular Collider (FCC) experiments, 3D pixel sensors have become indispensable components due to their superior radiation hardness, fast response, and low power consumption. However, there are still significant challenges in the process of 3D sensors manufacturing. In this work, single devices and arrays of 3D sensors based on 30 μm epitaxial silicon wafer have been designed, simulated, fabricated, and tested. This process was developed on the 8-inch CMOS process platform of the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS). The key processes include Deep Reactive Ion Etching (DRIE) with the Bosch process, in-situ doping, and an innovative back-etching. After testing the 3D pixel sensors, we have summarized the leakage current and capacitance of devices with different sizes with respect to bias voltages. We also found that the fabricated devices were almost all successfully produced, which laid a strong foundation for subsequent large-scale mass production.

Index Terms—3D pixel sensors, CMOS process platform, Deep Reactive Ion Etching (DRIE), in-situ doping, back-etching technology

I. INTRODUCTION

THE relentless pursuit of high-performance radiation detectors for particle physics experiments, medical imaging, and space applications has driven the evolution of semiconductor sensor technologies. Among these, the 3D pixel sensors proposed by S. Parker *et al.* in 1997 [1] represent a paradigm shift from traditional planar designs. In this design, electrodes penetrate the silicon substrate perpendicular to the surface. This approach offers superior radiation hardness [2], fast charge collection, and low power consumption. These

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advantages become particularly crucial for future collider experiments facing extreme radiation environments.

The RD50 collaboration pioneered systematic radiation tolerance studies of 3D sensors by establishing standardized testing protocols under high-fluence conditions [3], laying the foundation for their first large-scale application in the ATLAS Insertable B-Layer (IBL) project, marking the technology's successful deployment at the Large Hadron Collider (LHC) [4]. Research teams from the Barcelona Institute of Microelectronics (IMB-CNM) [5], [6], [7], Fondazione Bruno Kessler (FBK) [8], [9], [10], and SINTEF [11], [12], [13], [14] have also made significant breakthroughs in process innovation.

Despite these advancements, significant fabrication difficulties persist in 3D pixel sensors on production scale, including electrode shape control, aspect ratio, doping and filling processes, wafer flatness, mechanical stress, and warpage. The complex 3D electrode structures require advanced semiconductor processes, including deep reactive ion etching (DRIE) with the Bosch process [15] and in-situ doping. The intricate interplay between electrode geometry and electrical performance requires TCAD simulation-guided optimization [16]. Moreover, the long manufacturing cycle of 6 to 12 months and high costs further increase the development difficulty.

Fabrication of 3D sensors utilizing CMOS process is significantly important to large scale manufacture and integration to ASIC and readout circuit. To fulfill this, we designed and fabricated 3D pixel sensors on the 8-inch CMOS process platform in the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS). Fabricated 3D pixel sensors include single devices and array devices. We successfully developed a trench/column electrode structure with an aspect ratio of 70:1 (0.5 μm width), significantly increasing the sensor fill factor. This 3D trench/column structure effectively enhances the electrical insulation performance between adjacent pixels, while also featuring low depletion voltage and fast signal acquisition capability. The proposed 3D trench/column sensors are based on mature electrode theoretical frameworks [17], [18], that provide a reliable theoretical foundation for design. In this work, we will disclose more details of the fabrication process of 3D pixel sensors, providing a guarantee for large-scale production in the future.

The organizational structure of the remaining part of this paper is as follows: Section II elaborates in detail on the simulation process and results of single device of the 3D pixel sensors using the TCAD tool. Section III describes the designed fabrication process and key process innovations

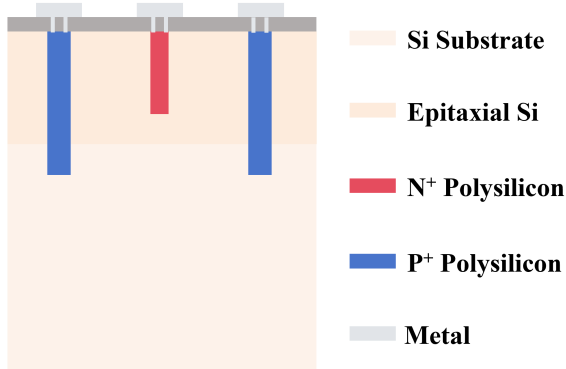


Fig. 1. Schematic of the single device structure.

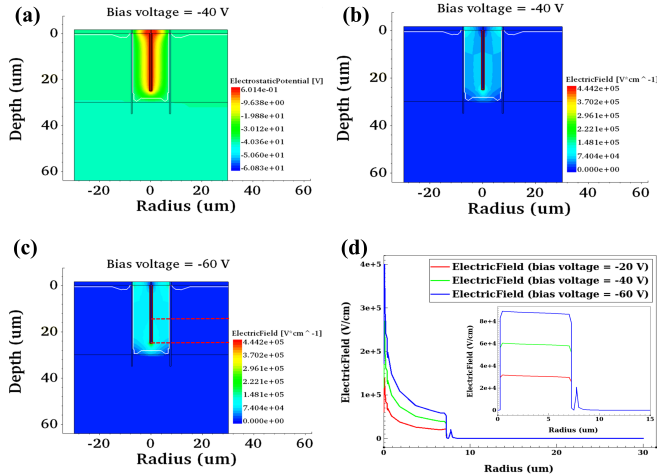


Fig. 2. (a) The potential distribution with a reverse bias voltage of 40 V. (b) The electric field distribution with a reverse bias voltage of 40 V. (c) The electric field distribution with a reverse bias voltage of 60 V. (d) The one-dimensional transverse electric field distribution at the depths of 25 μm and 15 μm for the device under different bias voltages.

with process details. Section IV presents leakage current and capacitance tests and analyses of the completed wafers, and then Section V presents a preliminary summary of this work with an outlook of future research directions.

II. DEVICE MODELING AND SIMULATION

Fig. 1 shows the 2D structure schematic of a single 3D sensor device. The device was fabricated on a 30 μm high-resistance epitaxial silicon, with the central column electrode doped with phosphorus at about 4×10^{20} atoms/ cm^{-3} . The side trench electrode that surrounding the central column electrode is doped with boron at about 2.8×10^{21} atoms/ cm^{-3} . The central column electrode is functioned as the collection electrode. The trench electrode is used to apply reverse bias voltage.

We used the TCAD tool to construct this structure and simulated the electric field and potential distributions of the device under different bias voltages. Fig. 2(a) and (b) show the electric field and potential distribution when the bias voltage is -40 V. Fig. 2(c) demonstrates the electric field when the bias

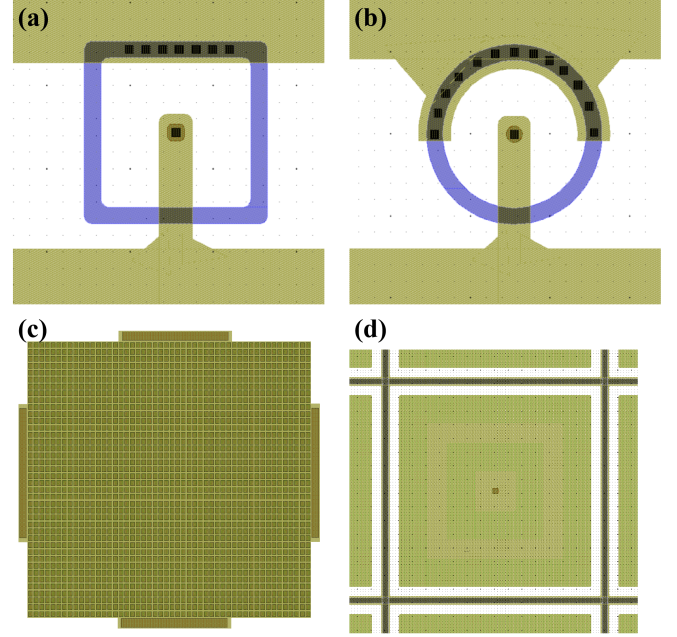


Fig. 3. Layouts of the (a) square single device, (b) circular single device, (c) array with a pixel size of 80 $\mu\text{m} \times 80 \mu\text{m}$, and (d) single device in the array with a pixel size of 80 $\mu\text{m} \times 80 \mu\text{m}$ of 3D pixel sensors.

voltage is -60 V. We found that as the bias voltage increases, the electric field in the depletion region of the device becomes stronger. Fig. 2(d) presents the electric field distribution at the bottom of the collection electrode, with an inset illustrating the electric field profile in the middle of the collection electrode. The exact location is shown by the dotted lines in Fig. 2(c). The analysis reveals a significant concentration of high electric field intensity adjacent to the bottom of the central collection electrode. It is attributed to the fact that the PN junction is located near the central electrode. By comparison, it can be seen that the electric field at the bottom of the central collection electrode is the highest. Under a 60 V bias, the electric field at the bottom of the collection electrode reaches 4×10^5 V/cm. It is sufficient to induce impact ionization and may lead to device breakdown, which is consistent with the subsequent test results.

Fig. 3 shows the layouts of two individual devices (square and circular) and the array with a pixel size of 80 $\mu\text{m} \times 80 \mu\text{m}$ of 3D pixel sensors. All our subsequent chip fabrication processes were carried out based on these layouts.

III. FABRICATION PROCESS

We will take the single device shown in Fig. 4 as an example to introduce the basic fabrication processes of the 3D pixel sensors. First, we prepare a high-resistance epitaxial silicon wafer with an epitaxial thickness of 30 μm as shown in Fig. 4(a). Next, at the center of each device, we use DRIE with the Bosch process to create column with a width of 0.5–2 μm and a depth of 20–25 μm as shown in Fig. 4(b). We use the corresponding thickness of photoresist based on the feature size of the pattern. After the dielectric etching, the

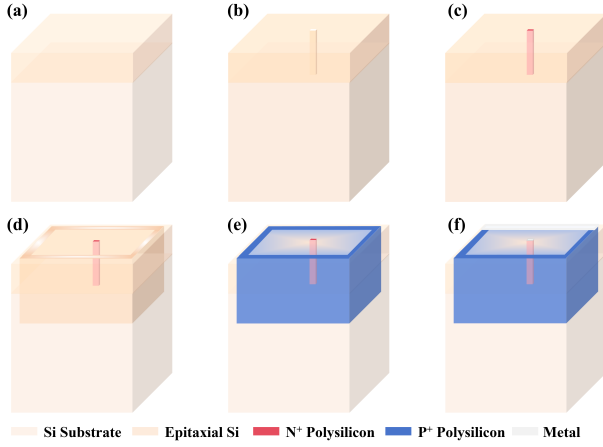


Fig. 4. Fabrication processes of the single device of 3D pixel sensors.

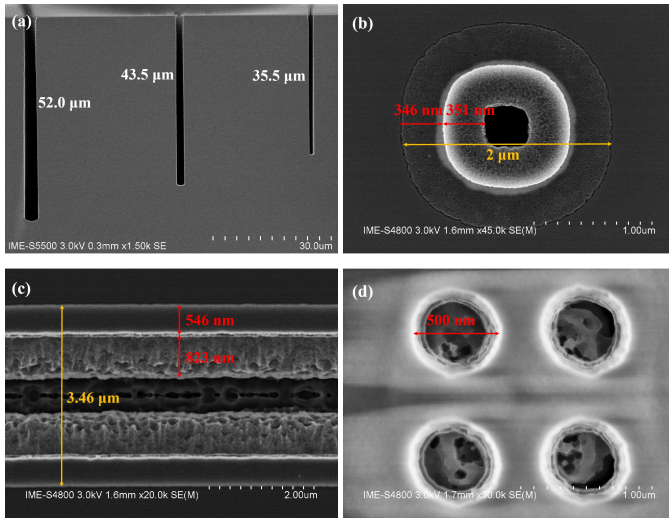


Fig. 5. The images of the trenches of 3D pixel sensors by using ultra high resolution scanning electron microscope (S-5500). (a) Etching depth corresponding to different trench/column width under the same etching time. (b) Surface image of the back-etching process of polysilicon on the 3D electrode. (c) The cross-sectional view of the 3D trench after the back-etching process of polysilicon on the 3D electrode. (d) The surface image of the central electrode vias etching.

remaining photoresist and the oxide layer are utilized as a hard mask for deep silicon etching. Then, we used in-situ doping to dope it into an N-type as shown in Fig. 4(c). Similarly, at the periphery of each device, we used DRIE with the Bosch process to create surrounding trench with a width of 0.5–2 μm and a depth of 30–50 μm as shown in Fig. 4(d). Then, we use in-situ doping to dope it into a P-type as shown in Fig. 4(e). Finally, the fabrication is completed by making metal electrodes for contact as shown in Fig. 4(f).

Next, we will introduce the specific details of the fabrication processes. The 3D trench/column electrodes have high verticality after etching. This is because during the DRIE with the Bosch process, we always use an oxide layer or photoresist as a hard mask. The thickness of the hard mask should be set reasonably according to the number of etching cycles and the overall process flow. Moreover, for different

trench/column widths, the etching depth is different under the same etching time. Under the same etching time, the wider the trench/column width, the deeper the etching depth, as shown in Fig. 5(a) [19]. We obtain an aspect ratio of 70:1 when the trench/column width is 0.5 μm .

After 3D trench/column etching, doped polysilicon is deposited via Chemical Vapor Deposition (CVD) using phosphorus or boron as the dopant source. This is a doping technique carried out during the material growth process, which can avoid damaging the crystal structure. We usually refer to this as in-situ doping. To prevent short circuits, the surface polysilicon of the 3D electrode needs to be completely removed after deposition. We adopt the back-etching process with a high selectivity to stop at the oxide layer, ensuring that the electrode surface is clean and free of residue, while the polysilicon on the sidewalls of the 3D trench/column electrodes is retained. The SEM image of the surface after the back-etching process is shown in Fig. 5(b), and the SEM image of the side of the 3D trench/column electrode after the back-etching process is shown in Fig. 5(c). As can be seen from the picture, the surface is smooth and flat, which lays the foundation for the subsequent contact fabrication.

After completing the polysilicon back-etching process, we deposit and planarize an oxide layer to fill voids inside the polysilicon and seal surface openings. This step enhances the insulation between electrodes and prevents surface leakage, which is critical for improving the stability and reliability of the 3D pixel sensors. Subsequently, we use photolithography and development to transfer the via pattern onto the wafer and ensure that the developed vias align with the underlying polysilicon. Then, we used dry etching technology to remove the oxide layer areas that were not protected by the photoresist, thereby forming vertical vias. We also checked the results to confirm the exposure status of the polycrystalline silicon on the silicon wafer. As shown in Fig. 5(d), it is the SEM image after the via etching.

Before the metal deposition, we use hydrofluoric acid (HF) to remove the residual oxide on the surface of polysilicon and then deposit Ti/TiN. This can reduce the contact resistance and increase the adhesion between tungsten and the oxide layer. Then, we perform isotropic deposition of the tungsten film to completely fill the vias. Similar to the back-etching process of polysilicon, we use back-etching technology to remove excess tungsten after vias filling to prevent short circuits between P⁺ and N⁺ electrodes. After completing tungsten etching, we perform over-etching to further remove the underlying TiN and Ti layers, thereby finishing the back-etching process.

Fig. 6 shows the surface and side profiles of the trenches and columns in the 3D pixel sensors that have been completed. It can be seen that all the trenches and columns have been filled and the surface is smooth.

As shown in Fig. 7, the physical images of two types of IMECAS fabricated 3D pixel sensors with trench shapes are presented under microscope and Focused Ion Beam Microscope (FIB). The electrode is composed of polysilicon and metal. The anode marked in the figure is the power supply electrode, where a negative reverse bias voltage is applied. The cathode marked in the figure is the read-out electrode

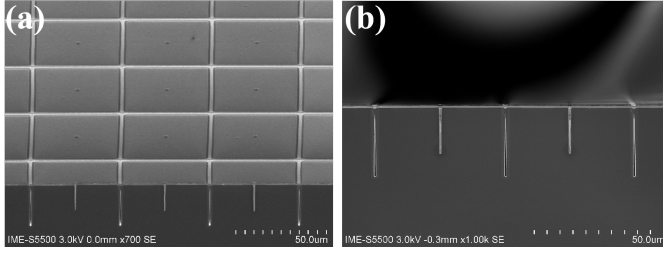


Fig. 6. (a) The overall view and (b) side view of the filled trenches and columns for the completed array.

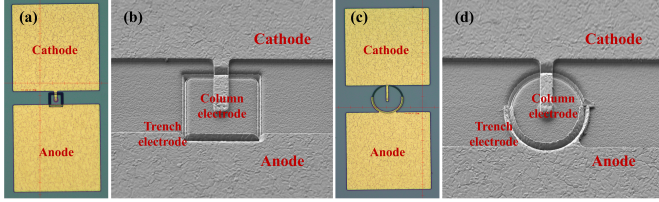


Fig. 7. (a) Microscope view and (b) Focused Ion Beam Microscope (FIB) view of the square shape of the single device of 3D pixel sensor. (c) Microscope view and (d) Focused Ion Beam Microscope (FIB) view of the circular shape of the single device of 3D pixel sensor.

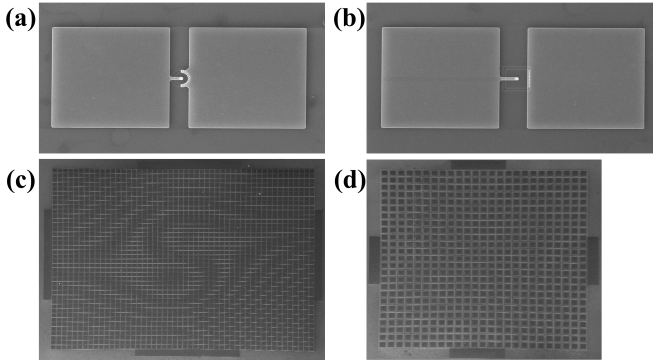


Fig. 8. The surface morphology of (a) the single device with circular shape, (b) the single device with square shape, (c) the array with pixel size of $150 \mu\text{m} \times 150 \mu\text{m}$, and (d) the array with pixel size of $80 \mu\text{m} \times 80 \mu\text{m}$ of 3D pixel sensors observed with Scanning Electron Microscope (SEM).

where a 0 V voltage will be applied during the test.

Fig. 8 presents the surface morphology of the single devices and arrays of 3D pixel sensors observed with Scanning Electron Microscope (SEM). The single devices of 3D pixel sensors in circular and square shapes are shown in Fig. 8(a) and Fig. 8(b) respectively. The array with pixel size of $150 \mu\text{m} \times 150 \mu\text{m}$ is shown in Fig. 8(c). The array with pixel size of $80 \mu\text{m} \times 80 \mu\text{m}$ is shown in Fig. 8(d). Here, we merely selected devices with different shapes for display. In fact, we have also pulled offsets of different sizes for devices of the same shape. We will summarize these parameters as well as the test results in the following tables (Table I and Table II).

IV. MEASUREMENTS AND ANALYSIS

As summarized in Table I, we can see geometry parameters and I-V/C-V results of four different arrays of 3D pixel sensors. The I-V and C-V curves are shown in Fig. 9(a) and

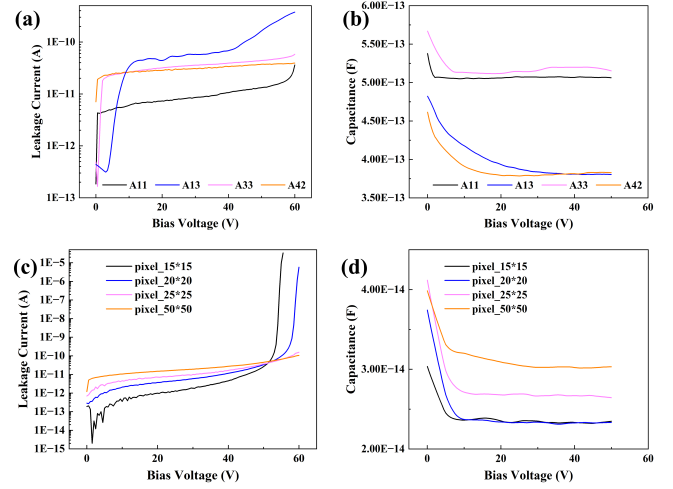


Fig. 9. The test results of the arrays and single devices of 3D pixel sensors. (a) The curves of leakage current of four arrays of 3D pixel sensors as a function of voltage. (b) The curves of capacitance of four arrays of 3D pixel sensors as a function of voltage. (c) The curves of leakage current of four single devices of 3D pixel sensors with different pixel sizes varying with voltage. (d) The curves of the capacitance of four single devices of 3D pixel sensors with different pixel sizes varying with voltage.

Fig. 9(b). Through analysis of the measurement results, it is observed that sensor arrays featuring smaller pixel dimensions generally exhibit reduced leakage current. The capacitance is dependent on the width and the depth of the collecting electrode theoretically. The measured capacitance values range from approximately 300 fF to 500 fF. The comparatively low leakage current and small capacitance are attributed to the use of a thin epitaxial layer as well as innovations in the fabrication process.

Table II summarizes geometry parameters and I-V/C-V results of thirty-one different single devices of 3D pixel sensors. We selected four devices (DR1, DR6, DR11, and DL9) with the same shape and trench/column width but different pixel sizes to plot their I-V and C-V curves, as shown in Fig. 9(c) and Fig. 9(d). We observed that as the pixel size increased, the leakage current and capacitance of the single device also increased. By comparing DL9, DL10, and DL11 in Table II, we found that among those with the same shape and pixel size but trench/column widths of 0.5 μm, 1.0 μm, and 2.0 μm, the single device DL10 with a trench/column width of 1.0 μm had the lowest leakage current, whereas the capacitance increased with the trench/column width.

Furthermore, systematic analysis of the Table II reveals a distinct correlation between pixel sizes and leakage current characteristics in devices with 2 μm trench/column width. For smaller pixel sizes, such as $10 \mu\text{m} \times 10 \mu\text{m}$, $15 \mu\text{m} \times 15 \mu\text{m}$, $20 \mu\text{m} \times 20 \mu\text{m}$, $25 \mu\text{m} \times 25 \mu\text{m}$, and $35 \mu\text{m} \times 35 \mu\text{m}$, the single-device leakage current demonstrates significantly higher values. In contrast, devices with larger pixel sizes, such as $50 \mu\text{m} \times 50 \mu\text{m}$, $80 \mu\text{m} \times 80 \mu\text{m}$, and $150 \mu\text{m} \times 150 \mu\text{m}$, exhibit a remarkable reduction in leakage current by approximately 1 to 2 orders of magnitude when incorporating the 2 μm trench/column width configuration. This may be caused by

TABLE I
PARAMETERS OF THE ARRAYS OF 3D PIXEL SENSORS

Name	Pixel Size (μm^2)	Array Dimensions	Trench/Column Width (μm)	Leakage Current (A) @ 20 V	Capacitance (F) @ 20 V
A11	80 × 80	40 × 50	2.0	7.32×10^{-12}	5.06×10^{-13}
A13	150 × 150	40 × 50	1.0	4.29×10^{-11}	3.94×10^{-13}
A33	80 × 80	40 × 50	1.0	3.18×10^{-11}	5.12×10^{-13}
A42	150 × 150	40 × 50	2.0	2.84×10^{-11}	3.79×10^{-13}

TABLE II
PARAMETERS OF THE SINGLE DEVICES OF 3D PIXEL SENSORS

Name	Pixel Size (μm^2)	Shape	Trench/Column Width (μm)	Leakage Current (A) @ 20 V	Capacitance (F)
DL(1–5)	10 × 10	Square (DL1, 2, 3) Circular (DL4, 5)	0.5 (DL1) 1.0 (DL2, 4) 2.0 (DL3, 5))	DL1: 5.73×10^{-13}	DL1: 2.59×10^{-14} @ 20 V
				DL2: 1.15×10^{-12}	DL2: —
				DL3: 9.21×10^{-8}	DL3: 2.60×10^{-14} @ 5 V
				DL4: 1.62×10^{-12}	DL4: 2.27×10^{-14} @ 5 V
				DL5: 1.64×10^{-9}	DL5: 2.10×10^{-14} @ 10 V
DL(6–8)	35 × 35	Square	0.5 (DL6) 1.0 (DL7) 2.0 (DL8))	DL6: 1.04×10^{-11}	DL6: 2.52×10^{-14} @ 20 V
				DL7: —	DL7: 6.78×10^{-15} @ 20 V
				DL8: 2.26×10^{-9}	DL8: 1.25×10^{-14} @ 20 V
				DL9: 1.48×10^{-11}	DL9: 3.06×10^{-14} @ 20 V
				DL10: 3.59×10^{-13}	DL10: 3.08×10^{-14} @ 20 V
DL(9–11)	50 × 50	Square	0.5 (DL9) 1.0 (DL10) 2.0 (DL11))	DL11: 1.71×10^{-11}	DL11: 4.70×10^{-14} @ 20 V
				DL12: —	DL12: 5.05×10^{-14} @ 10 V
				DL13: 1.01×10^{-11}	DL13: 5.49×10^{-14} @ 10 V
				DL14: 4.87×10^{-11}	DL14: 1.82×10^{-12} @ 10 V
				DL15: —	DL15: 1.29×10^{-12} @ 10 V
DL(12–13)	80 × 80	Square	0.5 (DL16) 1.0 (DL15) 2.0 (DL14))	DL16: 1.64×10^{-11}	DL16: 1.26×10^{-12} @ 10 V
				DR1: 9.79×10^{-13}	DR1: 2.38×10^{-14} @ 20 V
				DR2: 1.65×10^{-12}	DR2: 2.82×10^{-14} @ 20 V
				DR3: 2.50×10^{-9}	DR3: —
				DR4: 5.02×10^{-10}	DR4: 3.38×10^{-14} @ 10 V
DL(14–16)	150 × 150	Square	0.5 (DR6) 1.0 (DR7, 9) 2.0 (DR8, 10))	DR5: —	DR5: 2.85×10^{-15} @ 10 V
				DR6: 3.70×10^{-12}	DR6: 2.33×10^{-14} @ 20 V
				DR7: 1.80×10^{-12}	DR7: —
				DR8: 6.05×10^{-8}	DR8: 1.97×10^{-14} @ 10 V
				DR9: —	DR9: 1.25×10^{-14} @ 10 V
DR(1–5)	15 × 15	Square (DR1, 2, 3) Circular (DR4, 5)	0.5 (DR11) 1.0 (DR12, 14) 2.0 (DR13, 15))	DR10: —	DR10: 1.63×10^{-14} @ 10 V
				DR11: 7.14×10^{-12}	DR11: 2.72×10^{-14} @ 20 V
				DR12: —	DR12: 1.78×10^{-14} @ 10 V
				DR13: 9.24×10^{-8}	DR13: —
				DR14: 3.64×10^{-12}	DR14: 2.97×10^{-12} @ 10 V
DR(6–10)	20 × 20	Square (DR6, 7, 8) Circular (DR9, 10)		DR15: 1.01×10^{-8}	DR15: 2.21×10^{-14} @ 10 V
DR(11–15)	25 × 25	Square (DR11, 12, 13) Circular (DR14, 15)			

the fact that for small pixels, surface current may become dominant.

solid foundation for the future large-scale production of 3D pixel sensors using the CMOS platform.

V. CONCLUSION

In this article, we have elaborated on the entire processes of designing, simulating, layouting, fabricating and testing of 3D pixel sensors. The performance evaluation results clearly demonstrate that the sensors fabricated at IMECAS exhibit outstanding characteristics, such as the leakage current of most 3D pixel sensors less than 10 pA at 20V, and the capacitance below 3 pF. These attributes are critical for applications in high-radiation environments such as the HL-LHC upgrades. It can be conclusively demonstrated that we have successfully realized functional 3D pixel sensors with high yield and performance uniformity. More importantly, the expertise acquired in key steps such as DRIE with the Bosch process of high-aspect-ratio holes, polysilicon electrode filling, and back-etching process has enabled proficient mastery of the core fabrication processes. This achievement marks an important milestone in the development of radiation sensor technology, and lays a

REFERENCES

- [1] S.I. Parker, C.J. Kenney, and J. Segal, “3D — a proposed new architecture for solid-state radiation detectors,” *Nucl. Instr. and Meth. A.*, vol. 395, no. 3, pp. 328–343, Aug. 1997, 10.1016/S0168-9002(97)00694-3.
- [2] J. Lange, G. Giannini, S. Grinstein, M. Manna, G. Pellegrini, D. Quirion, S. Terzo and D. Vázquez Furelos, “Radiation hardness of small-pitch 3D pixel sensors up to a fluence of $3 \times 10^{16} \text{ neq/cm}^2$,” *J. Instrum.*, vol. 13, no. 09, pp. P09009, Sept. 2018, 10.1088/1748-0221/13/09/P09009.
- [3] RD50 Collaboration “Radiation hard semiconductor devices for very high luminosity colliders,” CERN-LHCC-2005-037 and LHCC-RD-009, Dec. 2005. [Online]. Available: <https://cds.cern.ch/record/901855/files/lhcc-2005-037.pdf>.
- [4] A. Gaudiello, “ATLAS pixel IBL modules construction experience and developments for future upgrade,” *Nucl. Instr. and Meth. A.*, vol. 796, pp. 56–59, Oct. 2015, 10.1016/j.nima.2015.02.033.
- [5] G. Pellegrini, M. Manna, and D. Quirion, “3D-Si single sided sensors for the innermost layer of the ATLAS pixel upgrade,” *Nucl. Instr. and Meth. A.*, vol. 924, pp. 69–72, Apr. 2019, 10.1016/j.nima.2018.05.076.
- [6] S. Terzo, J. Carlotto, S. Grinstein, M. Manna, G. Pellegrini and D. Quirion, “Performance of radiation hard 3D pixel sensors for the upgrade of the ATLAS inner tracker,” *J. Phys.: Conf. Ser.*, vol. 2374, no. 1, pp. 012168, 2022, 10.1088/1742-6596/2374/1/012168.

- [7] L. Diehl, S. Argyropoulos, O. Ferrer, M. Hauser, K. Jakobs, M. King, F. Lex, G. Kramberger, U. Parzefall, G. Pellegrini, C. Schwemmbauer, and D. Sperlich, "Evaluation of 3D sensors for fast timing applications," *Nucl. Instr. and Meth. A.*, vol. 1065, pp. 169517, Aug. 2024, 10.1016/j.nima.2024.169517.
- [8] A. Zoboli, M. Boscardin, L. Bosisio, G.-F. Dalla Betta, C. Piemonte, S. Ronchin, and N. Zorzi, "Double-sided, double-type-column 3-D detectors: design, fabrication, and technology evaluation," *IEEE Trans.Nucl.Sci.*, vol. 55, no. 5, pp. 2775–2784, Oct. 2008, 10.1109/TNS.2008.2002885.
- [9] G. Giacomini, A. Bagolini, M. Boscardin, G.-F. Dalla Betta, F. Mattedi, M. Povoli, E. Vianello, and N. Zorzi, "Development of double-sided full-passing-column 3D sensors at FBK," *IEEE Trans.Nucl.Sci.*, vol. 60, no. 3, pp. 2357–2366, Jun. 2013, 10.1109/TNS.2013.2262951.
- [10] D.M.S. Sultan, G.-F. Dalla Betta, R. Mendicino, M. Boscardin, S. Ronchin and N. Zorzi, "First production of new thin 3D sensors for HL-LHC at FBK," *J. Instrum.*, vol. 12, no. 01, pp. C01022, Jan. 2017, 10.1088/1748-0221/12/01/C01022.
- [11] A. Kok, T.-E. Hansen, T. Hansen, G. U. Jensen, N. Lietaer, M. Mielnik, and P. Storås, "High aspect ratio deep RIE for novel 3D radiation sensors in high energy physics applications," *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, Orlando, FL, USA, 2009, pp. 1623–1627, doi: 10.1109/NSSMIC.2009.5402256.
- [12] A. Kok, M. Boscardin, G.-F. D. Betta, C. Da Via, G. Darbo, C. Fleta, T.-E. Hansen, J. Hasi, C. Kenney, N. Lietaer, M. Lozano, S. I. Parker, G. Pellegrini, and A. Summanwar, "Results from the first prototype of large 3D active edge sensors," *2011 IEEE Nuclear Science Symposium Conference Record*, Valencia, Spain, 2011, pp. 1319–1323, doi: 10.1109/NSSMIC.2011.6154334.
- [13] O. Dorholt, T. Hansen, A. Heggelund, A. Kok, N. Pacifico, O. Rohne, H. Sandaker, B. Stugu, Z. Yang, M. Bomben, A. Rummeler, and J. Weingarten, "Beam tests of silicon pixel 3D-sensors developed at SINTEF," *J. Instrum.*, vol. 13, no. 08, pp. P08020, Aug. 2018, 10.1088/1748-0221/13/08/P08020.
- [14] S. Terzo, M. Boscardin, J. Carlotto, G.-F. Dalla Betta, G. Darbo, O. Dorholt, F. Ficorella, G. Gariano, C. Gemme, G. Giannini, S. Grinstein, A. Heggelund, S. Huiberts, A. Kok, O. Koybasi, A. Lapertosa, M. E. Lauritzen, M. Manna, R. Mendicino, H. Oide, G. Pellegrini, M. Povoli, D. Quirion, O. M. Rohne, S. Ronchin, H. Sandaker, M. A. Abdulla Samy, B. Stugu, and L. Vannoli, "Novel 3D pixel sensors for the upgrade of the ATLAS inner tracker," *Front. Phys.*, vol. 9, pp. 624668, Apr. 2021, 10.3389/fphy.2021.624668.
- [15] R. Abdolvand and F. Ayazi, "An advanced reactive ion etching process for very high aspect-ratio sub-micron wide trenches in silicon," *Sensors and Actuators A: Physical*, vol. 144, no. 1, pp. 109–116, May. 2008, 10.1016/j.sna.2007.12.026.
- [16] J. Kalliopuska, S. Eränen, and R. Orava, "3D simulations of 3D silicon radiation detector structures," *Nucl. Instr. and Meth. A.*, vol. 568, no. 1, pp. 27–33, Nov. 2006, 10.1016/j.nima.2006.07.015.
- [17] Z. Li, "New BNL 3D-Trench electrode Si detectors for radiation hard detectors for sLHC and for X-ray applications," *Nucl. Instr. and Meth. A.*, vol. 658, no. 1, pp. 90–97, May. 2011, 10.1016/j.nima.2011.05.003.
- [18] M. Liu, S. Lu, and Z. Li, "Theoretical bases of hypothetical sphere-electrode detectors and practical near-sphere-electrode (semisphere-electrode and near-semisphere-electrode) detectors," *J. Phys. D: Appl. Phys.*, vol. 54, no. 4, pp. 045101, Nov. 2020, 10.1088/1361-6463/abbe48.
- [19] M. Liu, H. Ji, W. Cheng, C. Liao, L. Zhang, Z. Li, B. Tang, P. Zhang, W. Xiong, T. Vickey, E. Giulio Villani, Z. Li, D. Zhang, and J. Luo, "Design, fabrication and initial test of a novel 3D-Trench sensor utilizing 8-inch CMOS compatible technology," *IEEE Trans.Nucl.Sci.*, to be published.